# DEVELOPMENT OF LOW-COST HIGH-EFFICIENCY COMMERCIAL-READY ADVANCED SILICON SOLAR CELLS

A Dissertation
Presented to
The Academic Faculty

by

Jiun-Hong Lai

In Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy in the
School of School of Electrical and Computer Engineering

Georgia Institute of Technology
August 2014

# DEVELOPMENT OF LOW-COST HIGH-EFFICIENCY

# COMMERCIAL-READY ADVANCED SILICON SOLAR CELLS

Approved by:


Dr. Ajeet Rohatgi, Advisor
School of Electrical and Computer Engineering
*Georgia Institute of Technology*

Dr. Gee-Kung Chang
School of Electrical and Computer Engineering
*Georgia Institute of Technology*

Dr. Thomas K. Gaylord
School of Electrical and Computer Engineering
*Georgia Institute of Technology*

Dr. Shreyes N. Melkote
School of Mechanical Engineering
*Georgia Institute of Technology*

Dr. Miroslav M. Begovic
School of Electrical and Computer Engineering
*Georgia Institute of Technology*


Date Approved: May 5th, 2014

*This thesis work is dedicated to my parents Mei-Hua Chen and Fu-Tien Lai, my brother Chun-Hsi (Kevin) Lai and my sister-in-law Mei-Yen (Sandy) Chiang, for their encouragement, support, and love.*

# ACKNOWLEDGEMENTS

I would like to express my sincere appreciation to my advisor Dr. Ajeet Rohatgi for supervising my Ph.D. study and providing the opportunity to conduct research in industry and academia. His advice on research and several collaborative experiences with industrial partners to solve existing problems allowed me to grow as a research scantiest. He has spent countless hours on guiding my research work and helping me to develop writing and presentation skills.

I would like to thank my committee members: Dr. Thomas K. Gaylord, Dr. Miroslav M. Begovic, Dr. Gee-Kung Chang, and Dr. Shreyes N. Melkote for serving as my committee members even in hardship. I would also like to thank Dr. Muhannad S. Bakir and Dr. James D. Meindl for their guidance and support in my first one and half years program at the Gigascale Integration (GSI) group.

I gratefully acknowledge the Suniva technical staff (Preston Davis, Liladhar Dahal, Julie Bixler, Linu Abraham, and Threa Tan) and the Suniva R&D staff (Dr. Daniel L. Meier, Bruce McPherson, Dr. Atul Gupta, Dr. Adam Payne, Dr. Vijay Yelundur, Dr. Arnab Das, Dr. Sheri X. Wang, Dr. Yi Wang, and Vinodh Chandrasekaran,) for their assistance in ion implantation and screen printing processes. I wish to thank Dr. Ernest Addo at PVCH, LLC for supplying the Aluminum conductor paste used in the phase one of this work. I would also like to thank Xudong Chen at nScrypt Inc. and Haixin Yang at DuPont Microcircuit Materials for their technical collaboration at the direct printing technology. I would like to thank Jeff Binns, Jesse Appel, Dr. Jason Guo, Dr. Hongbin Fang and Dr. Ethan Good at SunEdison Inc for their insightful technical discussions at

the collaboration of Indium doped material. I am grateful to Dr. Hang Chen for initially guidance and training in the process development of through silicon vias and sea of leads for 3-D interconnects at the GSI group.

I am truly grateful for past and present members of University Center of Excellence for Photovoltaics (UCEP) for their technical and emotional support through this process. I would like to offer my special thanks to Ajay Upadhyaya for his guidance during the early years of this work, to Keith Tate for initially training in the solar cell fabrication, to Dr. Arnab Das for many technical discussions and device modeling, to Dr. Saptharishi Ramanathan for sharing his expertise in small-area advanced solar cell fabrication, to Chai-Wei Chen for insightful discussions on solar cell physics and issues of silicon processing. I am especially grateful to James Keane, Kenneth Trotman, Ken Lamborn and Francesco Zimbardi for their extensive assistance with equipment maintenance and to Carla East for providing excellent administrative support. I am grateful for the support of the other UCEP members, including Dr. Abasifreke Ebong, Dr. Ian Cooper, Dr. Manav Sheoran, Dr. Young Woo Ok, Dr. Moon Hee Kang, Dr. John Renshaw, Brian Rounsaville, Vijaykumar Upadhyaya, Kyungsun Ryu, Malka Kadish, Eunhwan Cho, and Steven Ning.

I would like to express the deepest appreciation to Stephen Conover for being a good friend, roommate, and mentor throughout my Ph.D. years. I am particularly indebted to him for his numerous help and support whenever I am in need. He laughs with me at my best moments and stands by me at my worst moments. He helps me solve many difficulties during my student life and inspires me to become a better person. I will miss the countless Friday-night-dinners, movies, drinks, and the discussions of things

ranging from general to technical to the meaning of the life. I will cherish and carry my time with him over the years as memories forward with me. I would also like to offer my special thanks to Mrs. Sallie Conover and Mr. Dennis Conover for their kindly treatment to me like family. I will never forget my first authentic Thanksgiving in their warm house. Finally, I have greatly enjoyed my friendship with Daichi Tanaka, Dr. Aurèle Balavoine and Dr. Chris Turnes.

The research in this thesis was supported by the U.S. Department of Energy and the Silicon Solar Consortium (SiSoC).

# TABLE OF CONTENTS

# LIST OF TABLES

Page

# LIST OF FIGURES

Page

# LIST OF SYMBOLS AND ABBREVIATIONS

| | |
|---|---|
| $D_{it}$ | Interface state density |
| FF | Fill factor |
| $J_{01}$ | 1st diode reverse saturation current density |
| $J_{02}$ | 2nd diode reverse saturation current density |
| $J_{0b}$ | Base saturation current density |
| $J_{0b\text{-}met}$ | $J_{ob}$ in the metallized rear surface areas |
| $J_{0b\text{-}pass}$ | $J_{ob}$ in the passivated rear surface areas |
| $J_{0e}$ | Emitter saturation current density |
| $J_{0e\text{-}met}$ | $J_{oe}$ in the metallized emitter areas |
| $J_{0e\text{-}pass}$ | $J_{oe}$ in the passivated emitter areas |
| $J_{sc}$ | Short-circuit current density |
| $n_1$ | $1^{st}$ diode ideality factor |
| $n_2$ | $2^{nd}$ diode ideality factor |
| $Q_{ox}$ | Density of the fixed oxide charge |
| $R_b$ | Internal reflectance at rear surface |
| $R_s$ | Series resistance |
| $R_{sh}$ | Shunt resistance |
| S | Surface recombination velocity |
| $S_{eff}$ | Effective surface recombination velocity |
| $S_{n0}$ | Characteristic hole surface recombination velocity |
| $S_{p0}$ | Characteristic electron surface recombination velocity |

| | |
|---|---|
| $V_{oc}$ | Open-circuit voltage |
| $\Delta n$ | Injection level |
| $\delta_n$ | Hole capture cross-section |
| $\delta_p$ | Electron capture cross-section |
| $\eta$ | Energy conversion efficiency |
| $\tau$ | Minority carrier lifetime |
| $\tau_{eff}$ | Effective minority carrier lifetime |
| AM1.5G | Air mass 1.5 global |
| AR | Antireflection |
| BSF | Back surface field |
| BSR | Back surface reflector |
| BSRV | Back surface recombination velocity |
| C-V | Capacitance-voltage |
| Cz | Czochralski |
| DCE | Dichloroethene |
| ECV | Electrochemical capacitance-voltage |
| EQE | External quantum efficiency |
| FSRV | Front surface recombination velocity |
| FZ | Float-zone |
| HIT | Heterojunction with intrinsic thin-layer |
| IBC | Interdigitated back contact |
| IQE | Internal quantum efficiency |
| I-V | Current-voltage |

| | |
|---|---|
| LBIC | Light beam induced current |
| LID | Light-induced degradation |
| PC1D | Name of one-dimensional device simulation program for personal computers |
| PCD | Phtoconductance decay |
| PECVD | Plasma enhanced chemical vapor deposition |
| PERC | Passivated emitter and rear cell |
| PERL | Passivated emitter and rear locally diffused |
| PV | Photovoltaics |
| QSS-PC | Quasi-steady state photoconductance |
| SCA | Surface charge analyzer |
| SEM | Scanning electron microscopy |
| Si | Silicon |
| $SiN_x$ | Silicon nitride |
| $SiO_2$ | Silicon oxide |
| SMIS | Secondary ion mass spectroscopy |
| SRH | Shockley-read-Hall |
| SRP | Spreading resistance profile |
| UV | Ultraviolet |

# SUMMARY

Growing concern about excessive use of fossil fuels due to the pollution and emission of greenhouse gases has prompted scientists across the globe to develop renewable energy alternatives. Photovoltaics (PV)—the direct conversion of sunlight into electricity—is one of the promising options for maintaining sustainable energy supply because of environmentally friendly and a non-polluting low-maintenance energy source. In spite of the many advantages of PV mentioned above, solar energy currently accounts for only less than 1% of the global energy portfolio for electricity generation. This is because the cost of electricity from PV remains about a factor of two higher than the fossil fuel (10¢/kWh) in many locations around the globe. Cost modeling suggests that 19% efficient modules (correspond to ~21% efficient solar cells) can produce electricity at less than 10¢/kWh, which is often defined as grid parity in the U.S. for many applications.

Silicon solar cells with full Al-BSF and efficiency in the range of 16-19% currently dominate the commercial market because of their simplicity, high-throughput, and lower manufacturing cost. However, this structure has serious limitations in achieving > 20% efficiencies due to high back surface recombination velocity (> 300 cm/s) at the p-$p^+$ interface and the low back surface reflectance (~65 %). In contrast, most higher efficiency cells (~21%) today usually require a higher number of processing steps and expensive tools which raise the manufacturing cost and defeat the goal of achieving grid parity.

The objective of the research in this thesis is to develop manufacturable high-efficiency Si solar cells at low-cost through advanced cell design and technological innovations using industrially feasible processes and equipment on commercial-grade Czochralski (Cz) large-area (239 $cm^2$) silicon wafers. This is accomplished by reducing both the electrical and optical losses in solar cells through fundamental understanding and applied research and demonstrating the success by fabricating large-area commercial ready cells with much higher efficiency then the traditional Si cells.

In Chapter 2, the fundamental physics and the current understanding of the optical and electrical loss mechanisms are reviewed. In Chapter 3, three of the highest efficiency Si cell concepts in the literature with efficiency approaching 25% including the interdigitated back contact (IBC) cell, the heterojunction with intrinsic thin-layer (HIT) cell, and the passivated emitter and rear locally diffused (PERL) cell are reviewed. The advanced design features in these cells which led to reduced optical and electrical losses are highlighted in this chapter. The focus of this research is to develop low-cost high-efficiency PERC/PERL-type cells with dielectric passivation and local BSF with minimum number of processing steps using manufacturing technologies available today.

In Chapter 4, at the start of this research, large area commercial ready cells with POCl3 diffusion emitter, full Al BSF and screen printed contact was fabricated with efficiency of ~18.3%. This was comparable to the best in commercial ready cells at that time (2009). Detailed characterization and PC1D device modeling were used to assess the loss mechanisms in these cells. Device modeling was then extended to establish a practical roadmap that can achieve ~21% efficiency. All the necessary material and device parameters were also quantified to obtain the efficiency target of 21%. Detailed analysis of the baseline cell indicated that we need to improve front surface recombination velocity (FSRV) from 65,000 to 10,000 cm/s, back surface recombination velocity (BSRV) from 400 to 100 cm/s, back surface reflectance (BSR) from 70% to 96%, and front shading loss from 8.3% to 5.5% to raise the efficiency from 18.3% to

21%. This required many technology developments and innovations. Our technology roadmap showed that these requirements can be met by selective emitter, back side planarization, improved dielectric passivation, improved back reflector, local rear contacts, and fine-line printing.

In Chapter 5, ion implantation was successfully implemented for the first time for fabricating selective emitter Si solar cells without introducing additional steps. This is because ion implantation was performed through a graphite mask to achieve high quality single side patterned diffusion without the need for external masking, phosphosilicate glass (PSG) removal, and laser edge isolation. Early Learning Tool (ELT) as well as the first commercial implanter (Solian tool) for PV applications from Varian Semiconductor Equipment Associates was used in this research. The heavy and lightly doped regions can be formed in a single implant step directly on one side of the wafer using an appropriate shadow mask for implantation followed by a single high temperature anneal. This reduces processing cost while providing improved blue response and lower emitter saturation current density. Implantation conditions were tailored to achieve ~100 Ω/sq sheet resistance in the field and ~50 Ω/sq underneath the grid area. The ion-implanted selective cell structure gave 14 mV higher $V_{oc}$, 0.3 mA/cm$^2$ higher $J_{sc}$ and 0.5 % higher efficiency compared to the traditional $POCl_3$ diffused cell (18.3%). Detailed cell analysis and model calculations revealed that the ion-implanted selective emitter significantly lowered the $J_{oe}$ from 559 fA/cm$^2$ to 162 fA/cm$^2$, while the $J_{ob}$ of the full Al-BSF baseline structure stayed at 626 fA/cm$^2$, which limited the cell $V_{oc}$ and performance.

In Chapter 6, a more advanced cell structure was developed with passivated and local rear contacts (PERC cell) to drive the efficiency toward 21%. This chapter highlights the importance and optimization of wet chemical etching process for the rear side planarization, which was studied as a function of surface roughness, light trapping and surface passivation quality. The second part of this chapter addresses the optimization of the oxide thickness and its correlation with surface roughness, which was

examined by implied $V_{oc}$, oxide charge ($Q_{ox}$) and interface state density or quality (IQF) measurements. This was crucial for eliminating the rear parasitic shunting caused by inversion layer formation which can short or connect the local rear contacts. It was found that the rear dielectric layer not only needs to provide high quality passivation but should also contain a moderate positive charge density or a high negative charge density to avoid the formation of an inversion layer underneath the oxide. In addition, formation of a high quality thick and uniform local BSF through the dielectric is also important for preventing the parasitic shunt. This is because BSF between the Al metal and Si tends to become thin around the contact. Finally, guidelines from a 2-D device model were used to optimize the design and spacing of rear point contacts to minimize the combined effect of resistive and recombination losses. This chapter shows quantitatively that the back surface finish, rear oxide thickness, dielectric charge and interface quality, and local BSF design, all play an important role in providing excellent back passivation without rear parasitic shunting. This know-how was applied to fabricate cells with all the optimized parameters, namely 0.205 μm surface roughness, 90 Å oxide thickness, and 130 μm wide square contacts with 500 μm spacing. This resulted in 19.6% efficient, 239 $cm^2$ screen-printed Cz Si solar cells with the $V_{oc}$ of 656 mV, $J_{sc}$ of 38.5 $mA/cm^2$ and FF of 77.8%. This rear dielectric passivation and contact scheme (90 A oxide/600 A SiN) improved the BSR value form 70% to 93% and lowered the BSRV from 310 to 130 cm/s relative to the 18.3% full Al-BSF reference cell. This was one of the highest efficiency screen-printed 239 $cm^2$ p-type LBSF Cz Si solar cell in 2011.

In Chapter 7, a novel fine-line direct printing technology was investigated which can provide narrow grid lines with high aspect ratio and reduce front shading loss to enhance solar cell efficiency. Using the novel nScrypt direct printing technology in conjunction with DuPont Solamet® PV17X Ag paste, another ~0.5% efficiency improvement was demonstrated over the commercial screen-printed cells. The improvement in efficiency came from decreased emitter shading (increased $J_{sc}$),

optimized grid design for high Fill Factor, reduced Ag/Si specific contact, and emitter sheet resistance losses. This resulted in higher FF, lower $R_S$ and higher $J_{sc}$. An aspect ratio of 0.69 was achieved with direct printing with a line width 55 µm, height of 38 µm, and a shadow loss of 5.8%. This contrasts with the aspect ratio of 0.28 for the commercial screen-printed contacts with the line width of 100 µm, height of 28 µm, and shadow loss of 7.6%. Detailed analysis of $R_s$ demonstrated that direct printed solar cells also have appreciably lower emitter sheet loss and gridline resistance compared to their screen-printed counterpart. The direct printed cells with 83 gridlines resulted in 20.2% efficient Cz cells with the $V_{oc}$ of 657 mV, $J_{sc}$ of 38.4 mA/cm$^2$ and FF of 80.0%. This GEN-I PERC was one of the highest efficiency screen printed 239 cm$^2$ p-type oxide/nitride passivated LBSF Cz Si cell in 2012.

In Chapter 8, we proposed the roadmap to 21% GEN-II PERC with a homogeneous high-sheet-resistance emitter by a combination of fundamental understanding of loss mechanisms, process and design optimization, technology innovation and complete large-area cell fabrication. Since nScrypt's direct printing technology is not yet ready for commercial use because of the need for a high throughput multi-nozzle tool, we decided to focus on commercially viable screen printing by implementing emerging Ag pastes, new screens with improved emulsion and narrow openings. We started with 100 µm lines in 2009 and at the start of Chapter 8 we were printing 80 µm, which helped in raising GEN-I cell efficiency to ~20%. This was the results of improved pastes and screens with finer openings. Five efficiency enhancements were investigated in this chapter to raise the efficiency to ~21%. In the first subtask, we switched from selective emitters to a high sheet resistance homogeneous emitter. Low-cost 100 Ω/sq homogeneous emitter with lower surface concentration and optimized anneal conditions was developed for attaining the target $J_{oe}$ of ~130 fA/cm$^2$. In addition, the passivation quality of in-situ grown thermal $SiO_2$ and PECVD $SiN_x$ AR coating on the homogeneous emitter was optimized by effective lifetime measurements on

symmetric test structure ($n^+$-Si-$n^+$). In the second subtask, the ion implantation dose was optimized to tailor surface concentration to reduce contact loss to 100 Ω/sq emitter and achieve higher fill factor. The third subtask deals with the technology enhancement associated with raising BSR to above 95%. This involved ray tracing simulations using Sunrays optical modeling program to establish the requirements (thickness and index) for oxide and nitride in the rear stack followed by experimental validation of the model. In the fourth subtask in this chapter, we developed a line contact geometry for local back contacts instead of point contacts in phase-I to enhance the rear contact quality, cell manufacturability and throughput of the UV laser machine. In the fifth subtask, attempts were made to improve traditional screen-printed contact technology to reduce shadow losses and increase aspect ratio in an effort to shrink the gap between screen printing and direct printing technology (Chapter 7). In the sixth subtask, ~21% PERC cells were fabricated and their light-induced degradation (LID) characteristics were examined. The best cell efficiency of 20.8% was achieved for the GEN-II PERC cell in this study. Integration of all the optimized parameters, namely ~90 Ω/sq homogeneous emitter, 80 Å oxide thickness, 75 µm wide rear line contacts with 1 mm spacing, 2000 Å thick $SiN_x$ on top of 80 Å oxide, and successful screen printing of 60 µm wide narrow gridlines gave 11 mV improvement in $V_{oc}$, 0.7 mA/cm$^2$ improvement in $J_{sc}$, 0.3 % in FF compared to the GEN-I screen-printed PERC cell with $V_{oc}$ of 656 mV, $J_{sc}$ of 38.3 mA/cm$^2$, FF of 79.2%. The 20.8% efficient PERC cell had $V_{oc}$ of 667 mV, $J_{sc}$ of 39.1 mA/cm$^2$, and FF of 0.798. This demonstrates that the fundamental understanding and various technology enhancements developed in this chapter were successfully in bringing the large-area screen printed PERC cell efficiency close to 21%. At the end of this study, light-induced degradation (LID) due to the formation of boron-oxygen (B-O) complexes in the bulk of p-type boron-doped Cz silicon cells was studied and quantified for the PERC and the baseline full Al-BSF cells fabricated in this study. The PERC cell showed ~0.8% loss in absolute efficiency, while the absolute efficiency of the baseline cell dropped by ~0.5%

after 72 hours of illumination. This agreed well with the modeling done by Das et al., which predicted greater loss for the PERC cells. To achieve higher stabilized efficiency for PERC cells either oxygen content need to be reduced or B dopant should be replaced by Ga or In.

In Chapter 9, we evaluated for the first time the efficiency potential and LID in In-doped PERC cell. For the first time, a 20% efficient large-area, screen-printed, In-doped, monocrystalline cell was fabricated in this research with no appreciable light-induced degradation. Conventional full Al-BSF baseline cells gave nearly identical efficiencies of ~19.1% for the In- and B-doped wafers. However, after ~0.7 sun, 72-hour illuminations, the In-doped cells showed negligible LID, resulting in much higher stabilized efficiency while the B-doped baseline cell efficiency dropped to ~18.6%. In-doped substrates gave a best PERC cell efficiency of 20.0% compared with 20.3% and 20.5% for the two B-doped sets grown in the similar Cz puller. However, after light exposure, the high oxygen (21 ppma) B-doped cell with efficiency of 20.4% showed ~1% loss in absolute efficiency while the other B doped wafer with 14 ppma oxygen gave an efficiency of 20.1% which dropped by ~0.6% due to LID. Again, the indium- doped PERC cell showed $\leq 0.1\%$ loss in absolute efficiency due to LID. Thus, in spite slightly lower starting efficiency, In-doped PERC cells showed much higher stabilized efficiency compared to their counterpart B-doped PERC cells. This shows the potential of In-doped cells for higher stabilized efficiency and energy production over the 30 years life of a module.

Last, Chapter 10 talks about the research directions to further improve the PERC. A technology roadmap for driving the PERC cell efficiency to 22% is developed in this chapter. This introduces three technology developments (1) use of selective emitter (150/85 Ω/sq) in conjunction with fine line double printing technology which can print ~40 μm lines, (2) use of low resistivity (1 Ω-cm) and high lifetime (~2 ms) p-type Si

wafers, and (3) higher quality front and back passivation layers which can produce BSRV of 10 cm/s and FSRV of 2000 cm/s.

In summary, this thesis developed a cost-effective, simple, and manufacturable process sequence to fabricate high-efficiency screen-printed PERC on industrial grade 239 $cm^2$ p-type Cz Si wafers using commercial ready technologies and equipment. This innovative low-cost process sequence features ion-implanted emitter, single high-temperature anneal step, optimized dielectric surface passivation, AR coating, rear reflector, fine line screen-printed metallization on front, and optimized line contact geometries on the back side. The PERC cells fabricated with this process achieved 20.8% efficiency on commercial grad 239 $cm^2$ Cz silicon wafers compared to 18.3% industrial cell with full Al-BSF cells at the start of this thesis. This thesis also demonstrates for the first time, a 20% efficient large-area, screen-printed, In-doped, PERC cell with no appreciable light light-induced degradation. A roadmap for attaining 22% PERC cells is developed in the thesis to guide the future research on this topic

# CHAPTER 1

# INTRODUCTION AND RESEARCH OBJECTIVES

## 1.1 Statement of the Problem

At present, more than 85% of the world's energy supply comes from fossil fuels: coal, oil, and natural gas (Figure 1.1) [1]. Nuclear and renewable energy account for the remaining 15% of energy needs. The projections are that the global energy demand will increase about 50% between 2011 and 2035 [1] as a consequence of industrial development and population growth. The high usage of fossil fuels is primarily because they can generate electricity more cost effectively today than the alternatives. However, there is growing concern about excessive use of fossil fuels due to the pollution and emission of greenhouse gases (carbon dioxide, methane, and nitrous oxide) that have been linked to climate change. Evidence shows that the use of fossil fuels has led to a steady rise in the temperature of the earth since the Industrial Revolution in the $20^{th}$ century (Figure 1.2) [2]. Business as usual can have very detrimental impact on our environment and can lead to depletion or shortage of oil supply in the near future. This, combined with the rapidly increasing energy demand, will significantly increase the global prices of petroleum products. Although nuclear energy is a potential candidate for reducing global warming, it poses a threat of nuclear accidents similar to Fukushima Daiichi and Chernobyl. All of these concerns about the fossil fuels and nuclear energy have prompted scientists across the globe to develop renewable energy alternatives including photovoltaics, which is the focus of this research.

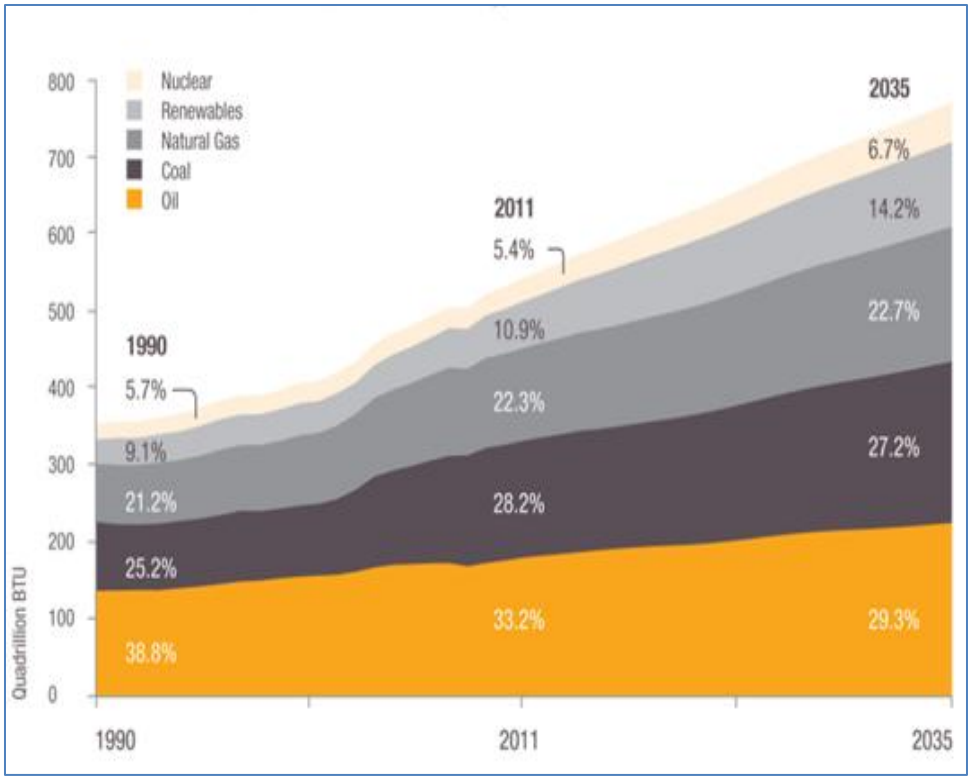



**Figure 1.1 Global energy usage and future demand [1].**

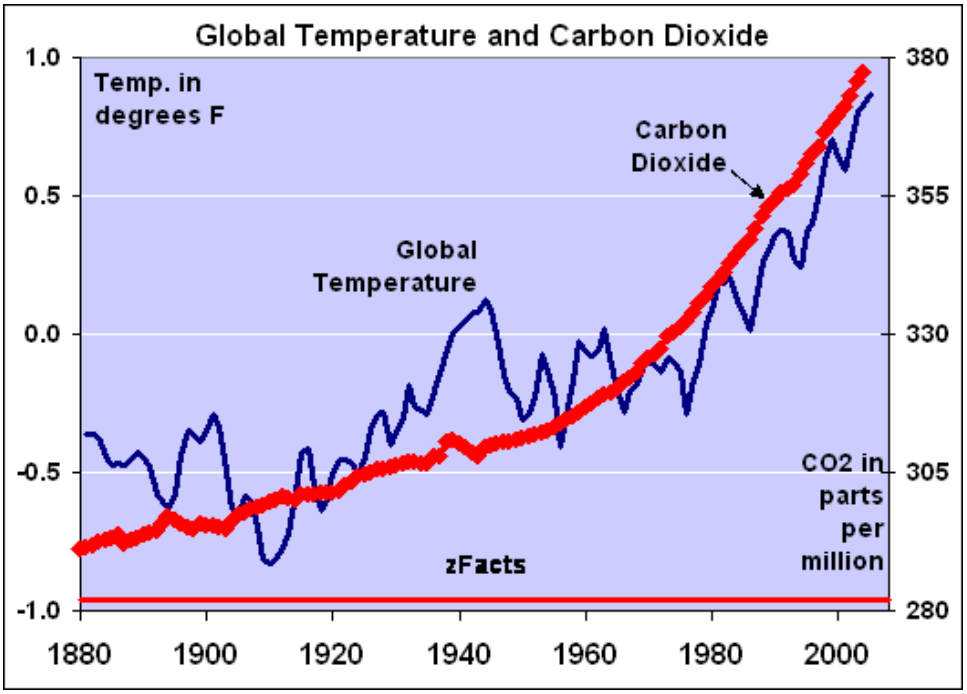



**Figure 1.2 Global temperature and carbon dioxide [2].**

Renewable energy is generally defined as energy that comes from natural resources that are essentially inexhaustible—such as sunlight, wind, hydropower, geothermal, and some forms of biomass. These resources are naturally replenished at a faster rate than they are consumed. Photovoltaics (PV)—the direct conversion of sunlight into electricity—is one of the promising options for maintaining sustainable energy supply because it is an environmentally friendly and a non-polluting low-maintenance energy source. The promise of PV as an energy source is further enhanced by the fact that sunlight is free, abundant, and not localized in any part of the world as shown in Figure 1.3 [3]. The annual amount of solar radiation reaching Earth's surface is ~$3.8 \times 10^{24}$ J, which is about 10,000 times more than the global annual energy consumption (~$5 \times 10^{20}$ J) [1]. Just one hour of sunlight falling on the Earth provides more energy than the entire world's needs in one year. The International Energy Annual (IEA) solar PV roadmap projects that PV will provide ~11% of global electricity by 2050, which will result in a reduction in $CO_2$ emissions by ~50% globally [4]. Therefore, PV will play an important role in meeting the anticipated growth in energy demand while reducing global greenhouse gas emissions.

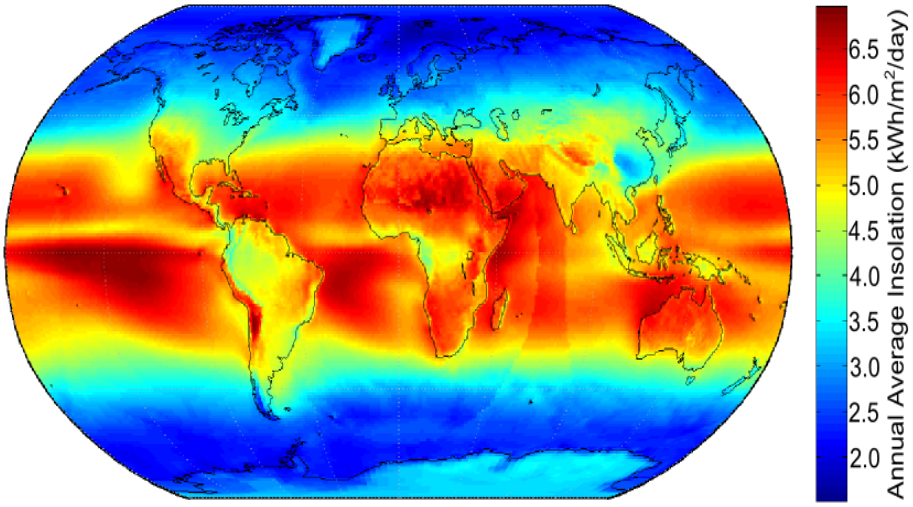



**Figure 1.3 Global map of insolation incident on a horizontal surface [3].**

In spite of the many advantages of PV mentioned above, solar energy currently accounts for only less than 1% of the global energy portfolio for energy generation as shown in Figure 1.4 [5]. This is because the levelized cost of electricity (LCOE) from PV (10-20¢/kWh) remains about a factor of two higher than the fossil fuel and nuclear powered electricity in many locations around the globe [6].

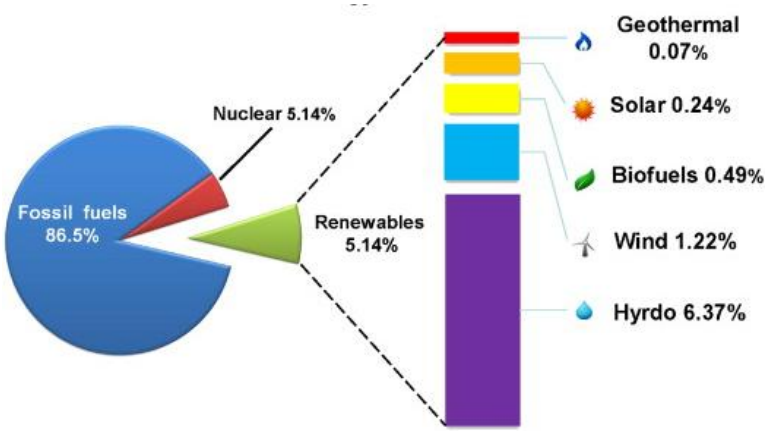



**Figure 1.4 Global energy consumption by source (2011) [5].**

However, in some locations, like Germany, Italy and Hawaii, etc., it is at or below grid parity. Cost modeling shown in Figure 1.5 suggests that 19% efficient modules at a module cost of ~$0.5/W in combination with a balance of system (BOS) cost of $2/W can produce electricity at ~10¢/kWh [7], which is often defined as grid parity in the U.S. for many applications. Nineteen percent efficient modules correspond to ~21% efficient solar cells because ~2% efficiency is lost today due to encapsulation losses and the difference in cell to module area. The real challenge is how to manufacture such high-efficiency cells at reasonable cost so that the PV modules can meet cost and efficiency targets simultaneously to attain grid parity which is defined as parity between the price of electricity from PV and market price of electricity from the grid in that location.

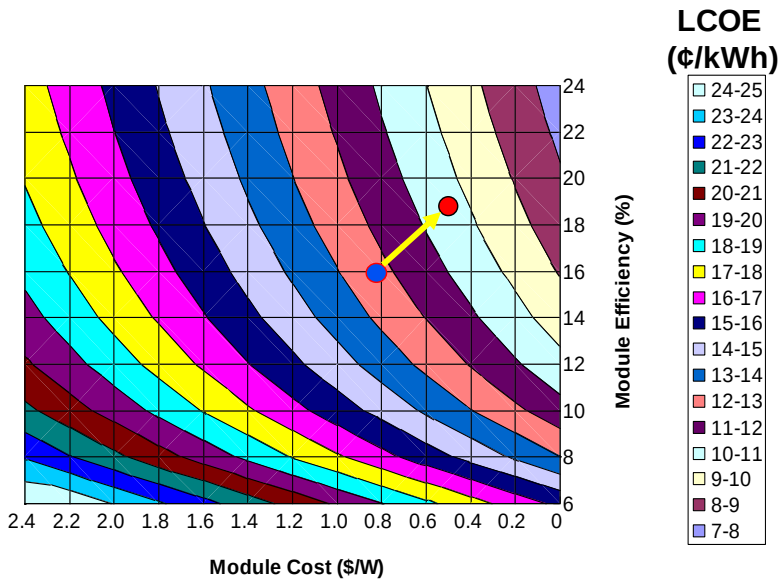



**Figure 1.5 LCOE contour plot for Atlanta area as a function of module cost and module efficiency with a BOS cost of $2/W [7].**

Currently, the PV market is dominated by silicon-based solar cells with cell efficiencies in the range of 16-19% depending on the cell structure, manufacturing technology, and Si wafer material quality. Solar cells with full-area screen-printed aluminum back surface field (Al-BSF) are most prevalent today (Figure 1.6) because of their design simplicity, high-throughput, and lower manufacturing cost.

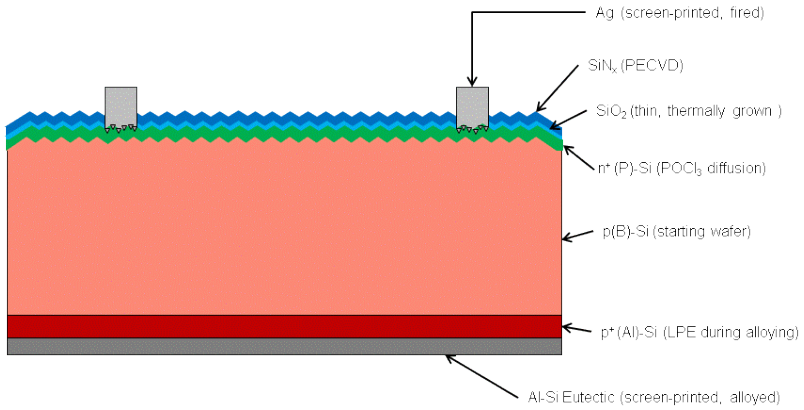



**Figure 1.6 A dominant commercial cell structure with a conventional POCl3 diffused emitter and full Al-BSF silicon solar cell.**

In contrast, higher efficiency cells (≥ 21%) today [8, 9] usually require a higher number of processing steps and tools which raise the manufacturing cost and defeat the goal of achieving grid parity. Therefore, the objective of the research in this thesis is to develop high-efficiency, low-cost Si solar cells through cell advanced design and technological innovations using industrially feasible processes and equipment on large-area (239 $cm^2$) commercial-grade Czochralski (Cz) silicon wafers.

## 1.2 Specific Research Objectives

Low-cost, high efficiency solar cells are the key to achieving grid parity with PV systems. Silicon solar cells with full Al-BSF and efficiency in the range of 16-19% currently dominate the commercial market because of their simplicity, high-throughput, and lower manufacturing cost. However, this structure (**Error! Reference source not found.**) has serious limitations in achieving > 20% efficiencies, especially on lower-cost thinner wafers. The disadvantages of a full Al-BSF cell include high back surface recombination velocity (> 300 cm/s) at the p-$p^+$ interface and the low back surface reflectance (~65 %), which limit the cell performance. In addition, a screen printed full Al-BSF warps the thin cells due to the difference in Si and Al expansion coefficient induced stress, presenting a barrier to using lower-cost thinner wafers for cost reductions. An alternative high-efficiency cell structure called PERL, passivated emitter and rear locally diffused (Figure 1.7), has been demonstrated on a laboratory scale to overcome the shortcomings of full area Al-BSF cells and produce ~25% cell efficiency [10]. However, cost effective production of such cells is impossible because of eight high temperature steps and four photolithography masks[11]. These cells are > 100 times more expensive than what is needed for grid parity. Thus producing high efficiency is not sufficient; reducing the production cost simultaneously is also critical which requires technological innovations, optimized cell design and use of low-cost commercial grade wafers and equipment. This provided the motivation for this research to develop an innovative low-cost manufacturable PERL or PERC cell, passivated emitter and rear cell (also called Delta-STAR in this thesis), by developing a low-cost process sequence that can boost commercial cell efficiencies close to 21% on large-area 239 $cm^2$ commercial grade Cz Si wafers using commercial ready equipment.

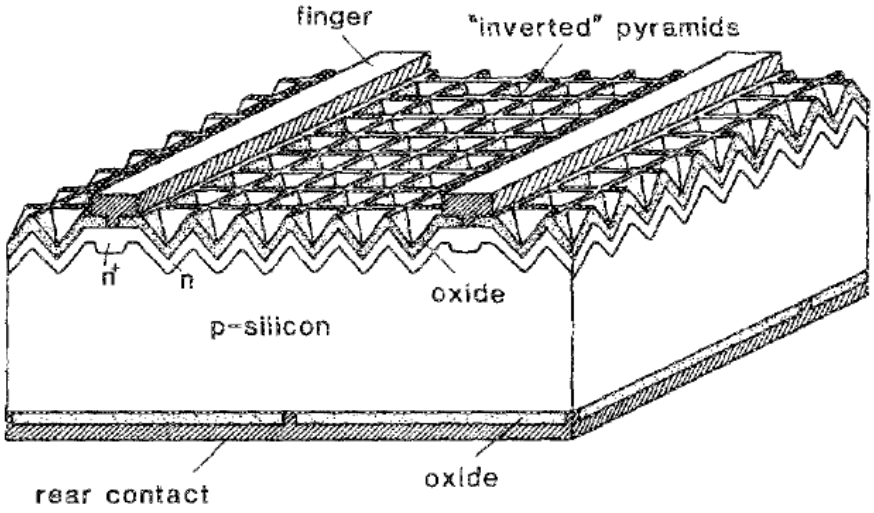



**Figure 1.7 Structure of high-efficiency of a PERC cell with passivated emitter and rear cell [10].**

The goal of simultaneously attaining the cost and efficiency targets of Si cell for grid parity will be accomplished through following seven tasks in this thesis.

**Task 1: Investigation of Selective Emitter Using a Novel Ion Implantation Technology**

Selective emitter is defined as a two tier emitter with heavy doping under the grid and light in the field. Ion implantation can simplify the fabrication of advanced solar cells because it allows the formation of high quality single side patterned diffusion and eliminates the non-value steps like masking, diffusion, less removal and laser edge isolation. Thus ion implantation can give higher efficiency and reduce cost simultaneously. This research will attempt for the first time on the use of ion implantation for fabrication of production ready large-area screen-printed ion-implanted high-efficiency (> 20%) PERC or Delta-STAR cells. Selective emitter formation can improve cell efficiency by reducing emitter recombination and contact resistance losses because heavy doping underneath the contact region improves the contact quality while lighter doping in the field (remaining portion of the emitter region) lowers emitter saturation

current density ($J_{0e}$) by reducing the heavy doping effects and improved surface passivation. A number of selective emitter technologies have been tried and reviewed in the literature [12]. Some of them are deployed on the current manufacturing line but the search for a more cost effective selective emitter technology is still ongoing because formation of selective emitter generally adds few additional processing steps. The objective of this task is to investigate and apply the ion implantation technology to achieve a high-quality selective emitter cost effectively by optimizing the dopant dose and energy without the need for double diffusion or patterning by masking and etching back. In addition, a high quality thermal oxide can be grown during the implant anneal, which can improve surface passivation at no additional cost. The decrease in emitter recombination losses in an oxide/nitride passivated, ion-implanted selective emitter cell will be compared with the widely used homogeneous $SiN_x$-passivated $POCl_3$ diffused emitter to quantify the benefit of ion-implanted selective emitter on $J_{0e}$ and cell efficiency.

**Task 2: Development of a Planarized Back Surface for High Quality Rear Side Passivation**

Single side planarization has been used in many high efficiency laboratory scale small-area (4 $cm^2$) float-zone (FZ) silicon solar cells. Planarization induced efficiency improvement over the traditional screen-printed full Al-BSF cells with back textured surfaces has been documented [10] and attributed to a low back surface recombination velocity (BSRV) and high back surface reflectance (BSR). Mechanical polishing gives the best planarization but it is too expensive for PV applications. Therefore, this task will study the impact of surface finish on cell efficiency and develop a low-cost single side chemical etching process that can lead to good passivation and high rear internal reflectance. The effect of planarization technique or process on surface roughness will be studied using confocal laser microscopy and long wavelength reflectance measurements.

The impact of surface roughness on passivation quality will be monitored by using the quasi-steady state photoconductance (QSS-PC) which measures cumulative recombination by providing effective lifetime and implied $V_{oc}$. A combination of planarizatoin process and oxidation will be developed and optimized to achieve best efficiency.

**Task 3: Development of a Dielectric Stack for Effective Rear Surface Passivation and Reflector**

Surface recombination is critical for high efficiency Si cells. Very low surface recombination velocities have been demonstrated on FZ Si wafers with thick thermally grown $SiO_2$ (~105 nm), plasma enhanced chemical vapor deposition (PECVD) of $SiN_x$, or a combination of both. Growth of such thick dry oxide and use of FZ Si wafers are not practical for mass production in solar cell industry due to low throughput and high cost. Therefore, the goal of the task is to investigate a thin thermal oxide grown in a mixture of dichloroethene (DCE) and oxygen ambient that can lower the process temperature and time without compromising the passivation quality. In addition, oxidation will be performed on commercial grade large-area Cz Si wafers (not on FZ Si) suitable for manufacturing. Another challenge will be to maintain the passivation quality or stability of this thin oxide during the high-temperature firing of screen-printed contacts which is done at the end of the cell process. Successful completion of this task is crucial for developing an industrially feasible, high efficiency, screen-printed PERC solar cells.

Another important objective of this task is to find a dielectric stack composed of thin $SiO_2$ and $SiN_x$ that can achieve high rear internal reflectance (> 95%). To accomplish this, ray tracing simulations will be performed using the software called Sunrays to gain quantitative understanding of the requirements (thickness and index) for each dielectric layer to achieve a high internal rear reflectance. Finally, various stacks of thin DCE oxides and $SiN_x$ layers will be grown and characterized to validate the model to achieve

high back surface reflectance. The results of this passivation and reflector studies will be applied to achieve higher efficiency PERC solar cells on commercial grade Cz Si wafers.

**Task 4: Design Optimization and Fabrication of Local Back Contacts through Dielectric Stack for High Efficiency PERC Cells**

PERC cells with dielectric back passivation need local BSF and contacts to Si through the dielectric stack. The design optimization of this contact scheme involves size and pitch local vias or lines. This can only be achieved by 2D device modeling. Meemongkolkiat [13] showed by 2D device modeling that the optimal back contact design is the result of the competition between the resistive and the contact recombination losses. This task will investigate various local contact designs to attain the right combination of rear contact size and pitch that will minimize the effective rear recombination velocity while maintaining low resistive losses. In addition, a rapid laser ablation technique will be developed to form local openings through the rear passivating dielectric instead of expensive and time-consuming photolithography used in the original R&D PERC cells. A UV laser will be used and laser parameters will be optimized including power and number of pulses required for adequate contact opening or size. The openings will be examined and optimized by optical microscopy. Finally, the impact of key contact parameters, such as pitch, size, shape (vias or lines) and the uniformity of the local Al-BSF, will be studied by scanning electron microscopy (SEM). This task is important for achieving > 20% efficient cells because uniform thick BSF is critical for lowering the effective BSRV and avoiding the formation of parasitic shunts.

**Task 5: Investigation of a Fine-Line Direct Printing Technology**

This task will implement a direct printing technology (without the need of a screen) developed by nScrypt corporation [14, 15] to form the front grid contacts with

reduced metal shading. This technology is somewhat like extrusion printing and can essentially write the front grid pattern on the wafer using a modified version of screen printable paste. It can form very fine gridlines with high aspect ratios to reduce shadow losses associated with the grid. However, reduction of gridline width can increase contact resistance and raise the sheet resistance loss to hurt the cell efficiency. Therefore, in this task the design of the grid pattern will be re-optimized using a grid modeling program to attain the full benefit of direct printing of fine line. Both conventional screen-printed and direct-printed cells will be fabricated to validate the model and achieve higher efficiency.

**Task 6: Development of Low-Cost High Sheet Resistance Homogeneous Emitter**

Selective emitter requires heavy doping under the grid lines for good ohmic contact and low doping in between the grid lines to reduce emitter recombination. In this study the selective emitter was formed initially in Task 1 by ion implantation through a shadow mask which played an important role in achieving higher efficiency PERC or Delta-STAR cells. However, the highly doped implanted wings or regions were ~500μm wide compared to < 100μm wide grid lines. This reduced the blue response of the cells due to higher surface and Auger recombination. Moreover, the selective emitter increased processing cost due to two different doping levels which requires an alignment to print gridlines onto the 500μm wide wings. Recently, new silver pastes have been developed by companies like DuPont and Heraeus which can enable ohmic contact to low-doped high sheet resistance emitters without significant increase in contact resistance. Therefore, in this task an implanted homogeneous high sheet resistance emitter will be developed with new Ag pastes to increase efficiency and lower cost simultaneously.

## Task 7: Light Induced Degradation Free PERC Cells on Indium Doped Silicon Material

It is well known that B-doped Cz Si cells show appreciable light induced degradation (LID) in absolute efficiency due to the formation of B-O complexes under illumination. Delta-STAR cell is more vulnerable to high LID loss because part of its efficiency enhancement comes from excellent back surface passivation. When LID reduces bulk lifetime, it decouples the back surface. Therefore, the impact of LID expected to be much greater on PERC cell because its efficiency degrades via bulk lifetime degradation as well as partial decoupling of the back surface passivation. This phenomenon can negate some of the benefit of PERC cell. However, there are few emerging alternatives to mitigate LID in PERC cell. Use of Si wafers with much less oxygen, or replacing boron (B) dopant by gallium (Ga), indium (In) or phosphorus (P). Some of these alternatives are being explored for conventional baseline cell designs. However, very little is known about In-doped Si. Therefore, this task will study and evaluate for the first time the cell performance and LID in large-area screen-printed high-efficiency PERC or Delta-STAR cells.

# CHAPTER 2

# FUDAMENTAL PHYSICS AND LOSS MECHANISMS OF SILICON SOLAR CELLS

Chapter two reviews the operating principles, the fundamental physics and the design considerations of silicon solar cells. It starts with the working principles of silicon solar cells based on the photovoltaic effect in a p-n junction under illumination followed by the fundamental physics and key parameters that dictate the performance of silicon solar cells. The last section deals with the loss mechanisms and the design considerations to achieve high-efficiency Si solar cells.

## 2.1 Working Principles of Solar Cells

A solar cell is a power delivering device that converts sunlight into electricity. The electricity generation from solar cells is based on a particularly designed p-n junction diode under illumination. The process of converting sunlight into voltage or electrical energy using solar cells is called photovoltaic effect that incorporates following three basic steps:

(1) When sunlight strikes a semiconductor or solar cell, a large number of electron-hole pairs are created in the device through absorption of photons with energy greater than the bandgap of the semiconductor.

(2) The electron-hole pairs diffuse randomly and are then separated by electrical field inside the p-n junction.

(3) The electrons end up in the n-type semiconductor and the holes on the p-type side resulting in a charge separation or voltage across the junction that leads current flow into the external circuit or load.

Figure 2.1 illustrates a schematic of a Si solar cell and its basic operation. The fabrication of current baseline type commercial cell involves formation of a p-n junction on the front side, a silicon nitride ($SiN_x$) anti-reflection coating (ARC) on the emitter surface, screen-printed silver (Ag) grid lines on the front side and full-area aluminum (Al) on the rear side. During a short high-temperature contact firing process, the Ag grid makes electrical contact on the front and Al dopes the silicon to form a $p^+$ Al back surface field (BSF) and contact on the rear. The BSF provides moderate passivation and optical reflection on the rear side of the cell. Currently, most commercial solar cells use screen-printing technique to form the front and back contacts because of simplicity, high-throughput, and low manufacturing cost. However, as mentioned before, this baseline cell has serious limitations to attain > 20% efficiency, which is the target of this research. Loss mechanisms in baseline cells and design of a more advanced PERC cell with dielectric back passivation and local BSF will be discussed in Chapter 3.

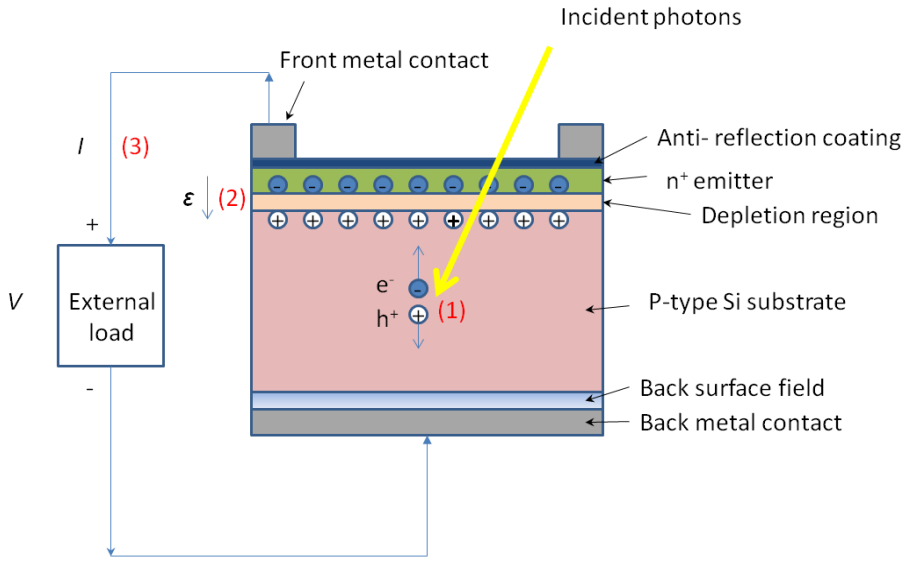



**Figure 2.1 A schematic of a simple solar cell structure showing (1) the generation of electron-hole pairs, (2) the separation of electron-hole pairs by the internal electrical field across the p-n junction and (3) the electrical current flowing through an external circuit.**

## 2.2 Fundamental Physics of Solar Cells

### 2.2.1 An Ideal Solar Cell and Its Equivalent Circuit

An ideal cell is modeled by a circuit with a current source connected in parallel with a p-n junction diode. Figure 2.2 shows the equivalent circuit of the ideal solar cell. In Figure 2.2, the current source represents the photo-generated current and the diode represents the solar cell in dark. This diode is characterized by a reverse saturation current density, $J_{01}$, and an ideality factor, $n_1$. The reverse saturation current density incorporates several key material properties (e.g. doping concentration, bandgap narrowing, Auger coefficient, diffusion length, and bulk lifetime) and process related parameters (e.g. emitter profile, front and back reflectance, and surface passivation quality). The detail expression of the $J_o$ will be discussed in the next section. The ideality factor describes how closely the diode follows an ideal diode behavior. The ideal diode assumes all the recombination occurs in the bulk region of the device (not in the junction region) and its ideality factor is one. In practice, recombination can also occur in the p-n junction region and cause the deviation from the ideal behavior. The ideality factor is generally greater than one in real diodes (1< n <2).

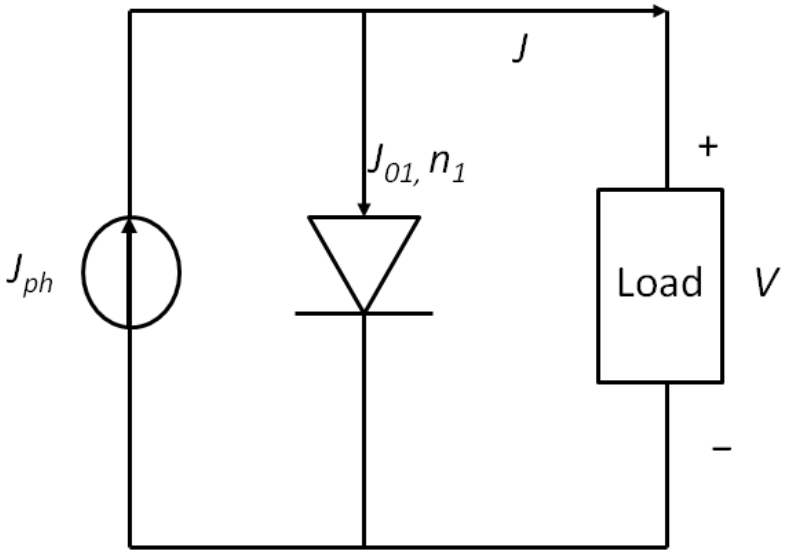



**Figure 2.2 Equivalent circuit of an ideal solar cell.**

### 2.2.2 Solar Cell under Dark

A solar cell under dark essentially behaviors like a p-n junction diode. The dark current density of the cell, $J_D$, can be expressed by the Shockley diode equation [16]:

$$J_D = J_0(e^{\frac{qV}{nkT}} - 1) \tag{2.1}$$

where $J_0$ is the reserve saturation current density, V the voltage across the terminals of the cell, n is the ideality factor, k is the Boltzmann constant, and T is the temperature.

For an infinite dimension p-n junction diode, the reserve saturation current density can be expressed as the following equation:

$$J_o = q(\frac{D_n}{L_n}\frac{n_i^2}{N_A} + \frac{D_p}{L_p}\frac{n_i^2}{N_D}) \tag{2.2}$$

where $D_n$ and $D_p$ are diffusion coefficients of electrons and holes, $L_n$ and $L_p$ are diffusion length of electrons and holes, and $N_D$ and $N_A$ are carrier concentrations of majority electrons and holes in n-type and p-type Si, respectively.

In practice, the dimension of a p-n junction diode is not infinite. This constraint modifies the expression of the reverse saturation current density $J_0$ to account for the recombination at the surfaces [17]:

$$J_o = J_{0e} + J_{0b} = q(\frac{D_n}{L_n}\frac{n_i^2}{N_A} \times F_p + \frac{D_p}{L_p}\frac{n_i^2}{N_D} \times F_n) \tag{2.3}$$

The $J_{oe}$ is the saturation current density contribution from emitter side and defined as recombination current density at the depletion edge on the emitter side. The $J_{oe}$ accounts for both the front surface recombination and bulk emitter recombination. The $J_{ob}$ is the saturation current density from base side. It is equal to the recombination current density at the depletion edge on the base side. $J_{ob}$ accounts for both bulk and rear surface recombination.

The $F_p$ and $F_n$ are called geometry factors and are expressed as:

$$F_n = \frac{\frac{S_p L_p}{D_p} + \tanh\left(\frac{W_p}{L_p}\right)}{1 + \frac{S_p L_p}{D_p}\tanh\left(\frac{p}{L_p}\right)} \quad (2.4)$$

$$F_p = \frac{\frac{S_n L_n}{D_n} + \tanh\left(\frac{W_n}{L_n}\right)}{1 + \frac{S_n L_n}{D_n}\tanh\left(\frac{W_n}{L_n}\right)} \quad (2.5)$$

where $S_n$ and $S_p$ are the surface recombination velocities of the electron and hole, respectively; $W_n$ and $W_p$ are the thickness of the emitter and the base, respectively.

It is interesting to note that if front and back surfaces are in contact with metal and their recombination velocities are very high ($S_p$ and $S_n \rightarrow \infty$), then $F_n$ and $F_P$ are reduced to:

$$F_n = \coth\left(\frac{W_n}{L_p}\right) \quad (2.6)$$

$$F_p = \coth\left(\frac{W_p}{L_n}\right) \quad (2.7)$$

On the other hand, if surfaces are very well passivated with $S_p$ and $S_n \rightarrow 0$, then $F_N$ and $F_P$ are reduced to:

$$F_n = \tanh\left(\frac{W_n}{L_n}\right) \quad (2.8)$$

$$F_p = \tanh\left(\frac{W_p}{L_p}\right) \quad (2.9)$$

It is important to note when $S > \frac{D}{L}, F > 1$, and $J_0$ increases. Reverse is true for $S < \frac{D}{L}$. Thus good surface passivation can lower $J_0$, which in turn can increase $V_{oc}$.

### 2.2.3 Solar Cell under Illumination

Illumination sends the diode into forward bias to trigger the dark current, $J_D$. In parallel, light generated carriers diffuse and get separated by the junction, resulting in

light-generated current $J_L$. According to the superposition principle, the total current (density) is expressed as the sum of the dark current and the photocurrent which flow in opposite directions. Graphically, dark I-V curve of a solar cell is shifted down by light generated current $J_L$ in the lower quadrant shown in Figure 2.3. Thus, the I-V equation of an ideal solar cell can be written as the following equation in the first quadrant (Figure 2.4):

$$J = J_L - J_0\left(e^{\frac{qV}{nkT}} - 1\right) \tag{2.10}$$

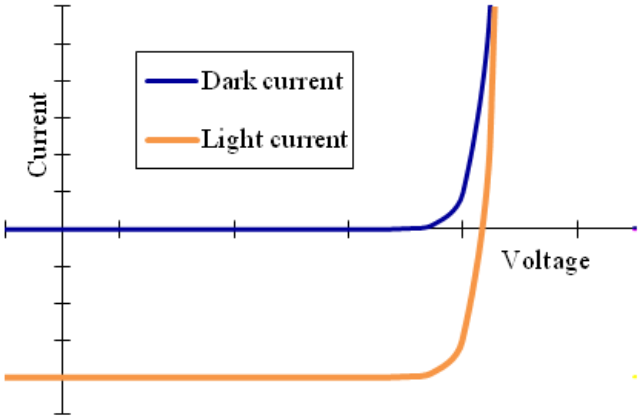



**Figure 2.3 I-V curve of a solar cell under dark and illumination.**

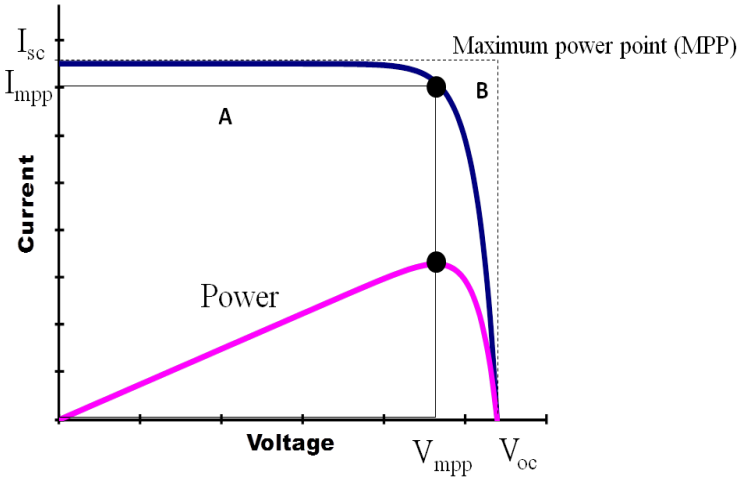



**Figure 2.4 I-V curve of a solar cell in the first quadrant.**

The photocurrent, $J_L$, is dictated by the incident solar spectrum and the spectral response of the cell. The spectral response at any wavelength (λ) is dictated by quantum efficiency (QE) which is the ratio of the number of carriers collected by the solar cell at that λ to the number of incident photons. If all the photons at a given wavelength are absorbed and resulting carriers are collected, then the external QE value will be 100% at that λ. In contrast, if the photons are partially reflected, transmitted, and/or recombined before they are collected by the cell, the QE will be less than 100%. There are two types of QE in the solar cell:

- External QE (EQE) includes the effect of surface reflectance and carrier collection losses.
- Internal QE (IQE) ignores the surface reflectance and accounts for only carrier collection or recombination in the cell.

The relation between EQE and IQE is expressed as:

$$EQE(\lambda) = \{1 - R(\lambda)\}IQE(\lambda) \tag{2.11}$$

where R(λ) is the percentage of light reflected from the surface of the cell.

The photocurrent is obtained by integrating the photo flux ($\phi(\lambda)$) from the highest photon energy to the cut-off energy (the bandgap energy of a material) and multiplying it by elementary charge ($q$) and EQE, which is given as:

$$I_L = q \int_{\lambda} \phi(\lambda)\{1 - R(\lambda)\}IQE(\lambda)d\lambda \tag{2.12}$$

To maximize the current in the cell, the cell design should confine most of the incident photons by minimizing the reflection and maximizing QE over the entire solar spectrum.

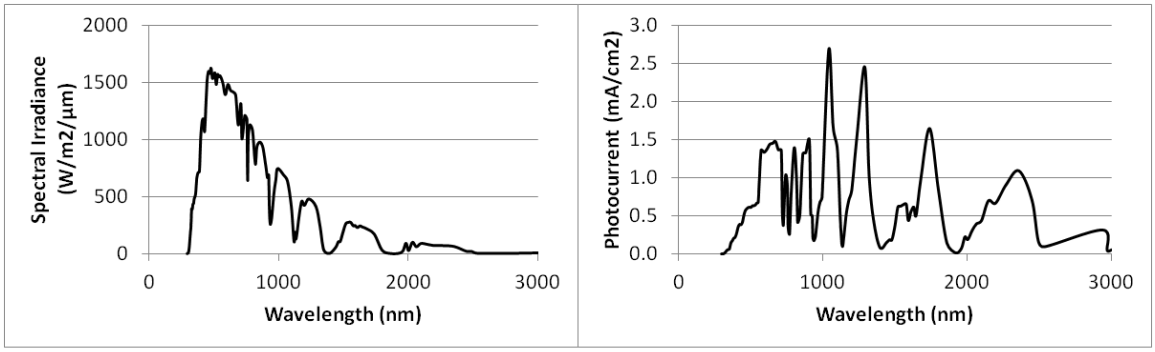
### 2.2.4 Cell Parameters and Their Upper Limits

The previous three sections discussed the operation of a p-n junction solar cell under dark and illumination. This section discusses the fundamental efficiency limiting parameters and their upper limits.

***Short-circuit current ($J_{sc}$)*** is the maximum current produced by a solar cell when the voltage across its terminals is zero (i.e. short circuit condition). Therefore, from Equation (2.10), $J_{sc}$ is given as:

$$J_{sc} = J_L \tag{2.13}$$

This equation indicates that the short-circuit current is equal to the photocurrent current, which is the result of generation and collection of light-generated carriers in the solar cell. To estimate the upper limits of short-circuit current in a Si cell, we can assume EQE equal to 100% and integrate the photon flux in the range of 300-1200 nm which is absorbed in silicon. Figure 2.5 shows the solar spectrum and its corresponding photocurrent at each wavelength. Sine silicon has a bandgap of 1.1 *eV*, it cannot absorb photons above $\lambda$ = 1.2 µm. Therefore, its maximum possible current density is about ~44 mA/cm$^2$ under standard AM1.5 illumination.




(a) (b)

**Figure 2.5 (a) Solar spectrum and (b) its corresponding photon current at each wavelength assuming 100% EQE.**

***Open-circuit voltage ($V_{oc}$)*** is when the cell current is zero and is the maximum voltage a solar cell can generate (i.e. open-circuit condition). By definition, an expression for $V_{oc}$ can be obtained from Equation (2.10) when $I = 0$. Thus, $V_{oc}$ is given as:

$$V_{oc} = \frac{nkT}{q} \ln \left(\frac{J_{sc}}{J_o} - 1\right) \tag{2.14}$$

Equation (2.14) indicates that the $V_{oc}$ depends on the short-circuit current and the reverse saturation current of the solar cell. The short-circuit current typically has a small variation while the reverse saturation current may vary by orders of magnitude. As shown in Equation (2.3), the saturation current is proportional to the total recombination in the solar cell. In other word, the open-circuit voltage is a measure of the amount of recombination in the cell. Therefore, to obtain maximum $V_{oc}$, the saturation current needs to be as low as possible. For silicon solar cell, the upper limits of $V_{oc}$ is about 785 mV when the total recombination is limited by Auger recombination in the bulk.

***Fill factor (FF)*** is a measure of the "squareness" of the I-V curve of the solar cell. It is the ratio of the maximum power output of a solar cell (area A in Figure 2.4) to the product of $V_{oc}$ and $J_{sc}$ (area B in Figure 2.4). The FF is given as:

$$FF = \frac{\text{Area A}}{\text{Area B}} = \frac{J_{mpp} V_{mpp}}{J_{sc} V_{oc}} \tag{2.15}$$

The FF is primary related to the resistive losses in a solar cell. However, some recombination mechanisms can also reduce the FF. The maximum possible FF can be expressed by an empirical equation below:

$$FF_o = \frac{v_{oc} - \ln (v_{oc} + 0.72)}{v_{oc} + 1} \tag{2.16}$$

where the $v_{oc}$ is defined as the normalized $V_{oc}$ and is given by the equation (2.17):

$$v_{oc} = \frac{V_{oc}}{\frac{nkT}{q}} \tag{2.17}$$

(2.15)

and n is the ideality factor. For a good solar cell, the FF can be above 0.80 or close to this value. For an ideal case with $V_{oc}$ = 785 mV, FF ≈ 0.860.

***Efficiency (η)*** is the product of $V_{oc}$, $J_{sc}$, and FF divided by the incident power. The energy conversion efficiency, η, is given by:

$$\eta = \frac{P_{mpp}}{P_{in}} = \frac{J_{sc} V_{oc} FF}{P_{in}} \tag{2.18}$$

where the $P_{in}$ is the incident power and $P_{mpp}$ is the maximum power output of a solar cell. The efficiency is typically measured under standard test conditions of AM1.5 spectrum with incident power density of 100 mW/cm$^2$, and at a temperature of 25˚ C. For the silicon solar cell, the theoretical maximum efficiency is about 29.3% with $V_{oc}$ = 785 mV, $J_{sc}$ = 44 mA/cm$^2$, FF = 0.860.

The efficiencies of commercial solar cells are only in the range of 16-19%, which are well below the theoretical limit due to many technological reasons and losses. Therefore, next section will review the loss mechanisms in solar cells with the objective of identifying the loss mechanisms that can drive Si solar cell efficiency close to 21% using commercial ready technologies and equipments.

## 2.3 Loss Mechanisms in Solar Cells

An essential part for achieving high-efficiency is the reduction of various losses in a solar cell. Understanding the loss mechanisms is the foundation for designing high-efficiency advanced solar cells. Since solar cell is an optoelectronic device, there are two major types of loss mechanisms in silicon solar cells: optical and electrical losses. Optical loss is referred to the loss of photons that could have generated electron-hole pairs in the cell. This loss reduces the short-circuit current and is attributed to front surface reflection, gridline shading and incompletely absorption of long wavelength light. Electrical loss is the photons that got absorbed in the cell but were not able to contribute to the cell power

output. This loss can reduce both short-circuit current and open-circuit voltage via carrier recombination and parasitic resistances. Figure 2.6 shows a schematic of various loss mechanisms in a solar cell. The following section discusses each loss mechanism in more detail followed by the design considerations for achieving high efficiency.

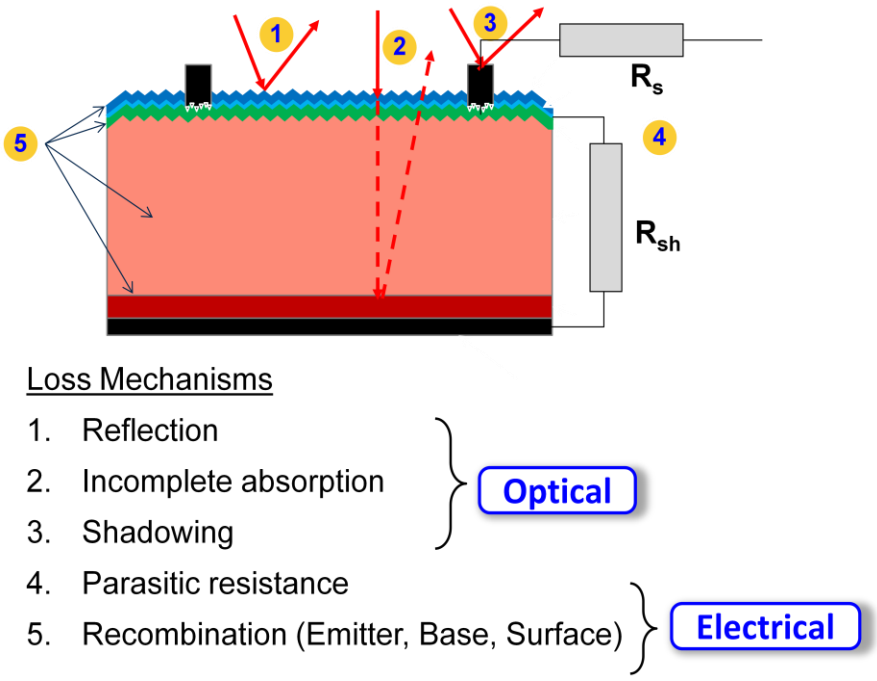



**Figure 2.6 Loss mechanisms in solar cells**

### 2.3.1 Reflection Loss

The reflection loss is attributed to a fraction of incident light reflected from the cell surface. A bare silicon surface reflects about 30% of the incident light because of the high refractive index of the silicon (n = 3.4). The surface reflection can be minimized by applying anti-reflection coating (ARC) and/or surface texturing on the front surface of the cell. The anti-reflection coatings are typically formed by dielectric layers with properly designed thicknesses and refractive indexes to produce destructive interference in the

rays reflected from the air-ARC interface and from the ARC-Si interface. Figure 2.7 illustrates the mechanism of an anti-reflection coating on the cell.

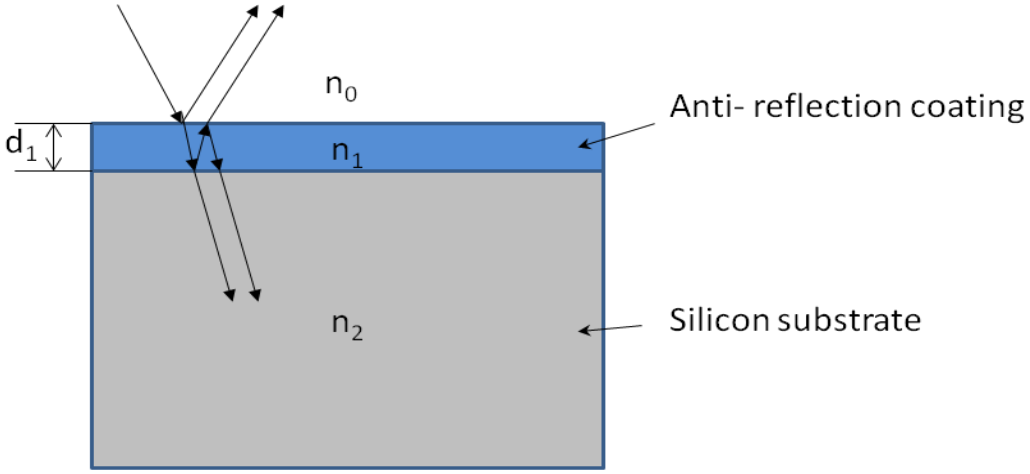



**Figure 2.7 Applying anti-reflection coating to reduce the surface reflection.**

The design principle of the anti-reflection coating is governed by optical quarter wave length and is captured in the formula is given by Equation (2.19).

$$n \cdot d = \frac{\lambda}{4} \tag{2.19}$$

where d is the thickness, n is the refractive index of the dielectric layer and λ is the wavelength.

For a single layer anti-reflection coating, the reflection at normal incident can be written in equation (2.15), according to Fresnel's formula.

$$R = \frac{r_1^2 + r_2^2 + 2r_1 r_2 \cos 2\theta}{1 + r_1^2 r_2^2 + 2r_1 r_2 \cos 2\theta} \tag{2.20}$$

Where

$$r_1 = \frac{n_0 - n_1}{n_0 + n_1} \tag{2.21}$$

$$r_2 = \frac{n_1 - n_2}{n_1 + n_2} \tag{2.22}$$

$$\theta = \frac{2\pi n_1 d_1}{\lambda} \tag{2.23}$$

where $n_0$ is the refractive index of the air, $n_1$ is the reflective index of the anti-reflection coating and $n_2$ is the refractive index of the silicon.

Using the quarter wave length principle, the minimum reflection is obtained by:

$$R_{min} = \left(\frac{n_1^2 - n_0 n_2}{n_1^2 + n_0 n_2}\right)^2 \tag{2.24}$$

The reflection becomes zero when

$$n_1 = \sqrt{n_0 n_2} \tag{2.25}$$

Note that the ARC design based on the Equation (2.24) gives minimum reflection only at a certain wavelength $\lambda$. The other wavelengths will not meet the condition of destructive interference. Therefore, the ARC design is typically designed to minimize the reflection between 500 nm to 600 nm where the solar spectrum has the maximum intensity.

A further reduce in reflection can be achieved by applying double-layer anti-reflection coating (DLARC). A common DLARC is formed by stacking zinc sulfide (ZnS) and magnesium fluoride ($MgF_2$) or titanium dioxide ($TiO_2$) and $MgF_2$. Figure 2.8 shows the reflection of bare silicon, single, and double layer anti-reflection coatings [18]. The DLARC reduces reflection in broader band of the solar spectrum and hence improves the solar cell efficiency. However, such DLARC process is too complex and expensive to implement on the commercial cells.

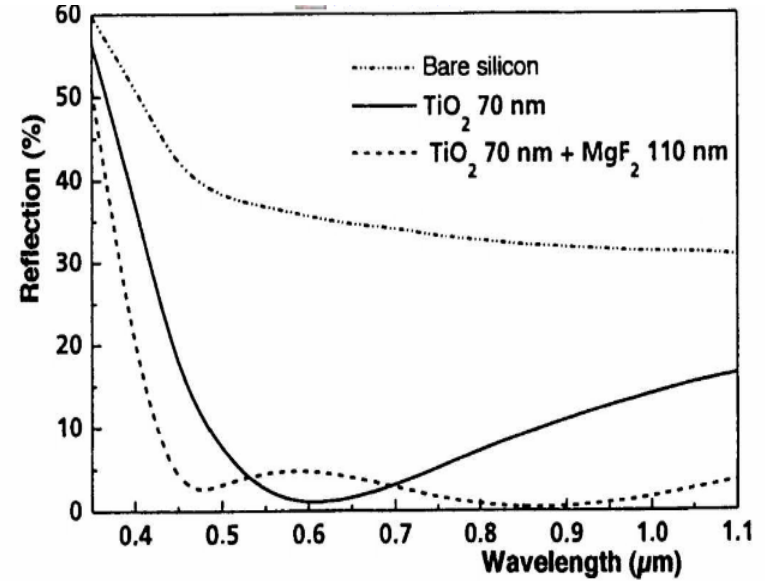



**Figure 2.8 Reflection of bare silicon with single and double layer anti-reflection coatings [18].**

### 2.3.2 Photon Loss due to Incomplete Absorption

The incomplete absorption happens for long wavelength photons that have enough energy to create electron-hole pairs but do not get absorbed in the cell due to insufficient optical path length in the cell. The optical path length is defined as the distance that light will travel within the cell before it escapes from the cell. The longer traveling distance or light trapping enhances the absorption of long wavelength light. Figure 2.9 (a) shows the absorption coefficient of silicon materials for different wavelengths. It reveals that the absorption coefficient drops significantly near ~1100 nm, which corresponds to the bandgap edge of silicon material. Figure 2.9 (b) shows the absorption depth in silicon, which is the inverse of the absorption coefficient. It clearly shows that a few centimeter thick of the silicon is required to completely absorb the long wavelength light. The loss due to incomplete absorption becomes more important when thin Si substrate is used for cost reduction.

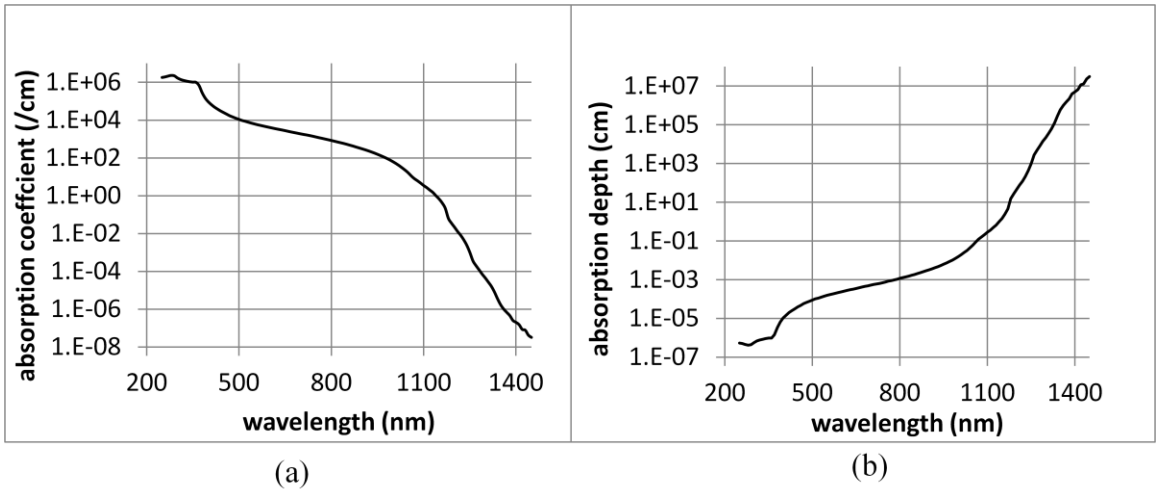



**Figure 2.9 (a) absorption coefficient of silicon; (b) absorption depth in silicon [19].**

This type of optical loss can be reduced by light trapping designs in solar cells. The light trapping by changing the angle of incident light or by allowing oblique penetration of light can increase the path length and enhance probability of absorption. A textured surface on the front surface can couple light obliquely inside the silicon material. Furthermore, when the light travels from high refractive index material to low refractive index material, the total internal reflection can occur at the rear surface if the incident angle is greater than the critical angle according to Snell's law. Consequently, the path length can be increased by a combination of front textured surface and rear reflector design. However, the textured surface increases the density of interface states which can increase surface recombination in the cell. Therefore, to mitigate the surface recombination, the light trapping is achieved by using a planar rear surface (keep front surface textured) to form a dielectric mirror that can reflect light back into the silicon. This will be discussed in more detail in Chapter 6.

### 2.3.3 Shading Loss

The contact to the front side of the commercial cell is typically made with metal fingers (or gridlines) which unfortunately prevent the light from entering the solar cell. This is referred to the shading loss. Both finger size and spacing are critical for cell performance because narrow fingers would allow more light to enter the solar cell but it will increase resistive loss because carriers have to travel longer distance to be collected by the grid. This trade off can be optimized by appropriate grid design using grid model in Chapter 7.

### 2.3.4 Resistive Loss

In a practical solar cell, the I-V characteristic usually differs from the ideal solar cell because of series resistance ($R_s$), shut resistance ($R_{sh}$) and recombination in the depletion region of the p-n junction. These are partly responsible for non-ideal behavior of a solar cell. Both resistive and recombination losses reduce the fill factor in the cell.

The resistive losses in a typical solar cell are associated with current travelling through the $R_s$(busbar), $R_s$(gridines), heavily doped emitter region $R_s$(sheet), metal-to-semiconductor contact on the front $R_s$(front contact), metal-to-semiconductor contact on the back $R_s$(back contact) and the Si substrate $R_s$(substrate) [20]. Figure 2.10 shows a schematic of the resistive components in a solar cell. The detail expression for the each resistive component is discussed in Chapter 7.

The quantitative impact of the series resistance on the FF is given by [17]:

$$FF = FF_o(1 - r_s) \tag{2.26}$$

where $FF_0$ is the ideal fill factor in Equation (2.16), with no $R_s$ and $R_{sh}$, $r_s$ is the normalized resistance ($R_s/R_{ch}$), and $R_{ch}$ is a characteristic resistance defined by $V_{oc}/I_{sc}$.

The $R_{sh}$ is typically due to process induced defects that provide an alternative path for the current. This reduces the amount of photocurrent flowing through the junction and reduces the voltage across the device. The impact of shut resistance can be expressed by:

$$FF = FF_o(1 - \frac{v_{oc} + 0.7}{v_{oc}}\frac{FF_o}{r_{sh}}) \qquad (2.27)$$

To assess the combined effect of $R_s$ and $R_{sh}$ , the $FF_0$ in Equation (2.27) is replaced by the fill factor in Equation (2.26).

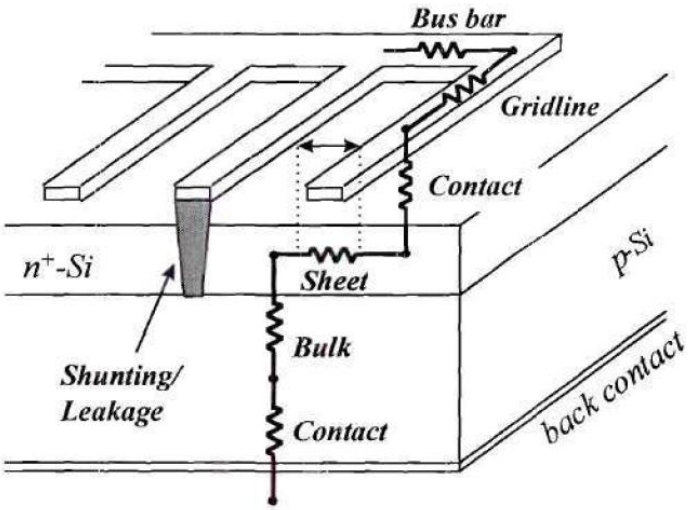



**Figure 2.10 Resistive components in a solar cell.**

### 2.3.5 Recombination Loss

When the light enters a solar cell, electron-hole pairs are generated throughout the device. Once the illumination is removed, the carrier concentrations will be naturally returned back to thermal equilibrium values via recombination of excess electron and hole pairs. There are four types of recombination process in a silicon solar cell:

1. Radiative recombination (or band-to-band recombination)
2. Doping induced Auger recombination
3. Defect induced Shockley-Read-Hall (SRH) recombination

4. Surface recombination

These recombination mechanisms occur simultaneously in the solar cell. The recombination rate (U) is characterized by bulk lifetime ($\tau$) defined as [21]:

$$\tau \equiv \frac{\Delta n}{U} \tag{2.28}$$

where $\tau$ is the minority carrier lifetime (s), U is the recombination rate ($cm^{-3}s^{-1}$) and $\Delta n$ is the excess carrier concentration ($cm^{-3}$). Note that the excess carrier concentration, also referred to as injection level, has significant influence on the recombination lifetime. Low level injection (LLI) refers to the condition where the number of excess carriers are small compared to the equilibrium doping concentration ($\Delta n$, $\Delta p << n_0$, $p_0$). High level injection (HLI) means that the number of excess carriers are large compared to the doping concentration ($\Delta n$, $\Delta p >> n_0$, $p_0$). Solar cell performance is a strong function of bulk lifetime; therefore, it is important to understand the fundamentals of recombination processes.

***Radiative recombination*** is also referred to as band-to-band recombination, reverse of the photogeneration in a semiconductor (Figure 2.11). In the radiative recombination, an electron in the conduction band directly annihilates a hole in the valance band and then releases the energy as a photon. This energy corresponds to the bandgap of the semiconductor. Radiative recombination is more significant in direct-band-gap semiconductors (e.g. GaAs) than in indirect ones (e.g. Si). This is because a phonon is required to conserve both energy and momentum in an indirect bandgap material.

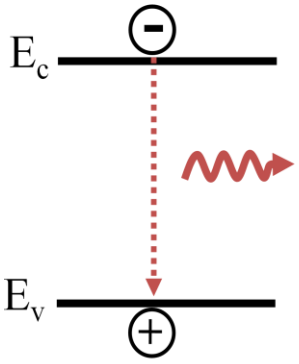



**Figure 2.11 Schematic illustration of radiative recombination.**

The radiative recombination rate, $U_{rad}$, depends on the electron concentration in the conduction band and the hole concentration in the valance band:

$$U_{rad} = B(np - n_i^2) \tag{2.29}$$

where B is the coefficient of radiative recombination, n is the electron concentration and p is the hole concentration. Radiative recombination lifetime is given by [22]:

$$\tau_{rad} = \frac{1}{B(n_0 + p_0 + \Delta n)} \tag{2.30}$$

, which reduces to $\tau_{rad,LLI} = \frac{1}{BN_{dop}}$ under low level injection and $\tau_{rad,HLI} = \frac{1}{B\Delta n}$ under high level injection, where $N_{dop}$ is the equilibrium doping concentration and $\Delta n$ is the injection level.

***Auger recombination*** is a three-particle process where an electron in the conduction band first recombines with a hole in the valance band and then transfers the excess energy to a third electron or hole (Figure 2.12). This third electron (or hole) then thermally relaxes back to its original energy by emitting phonon.

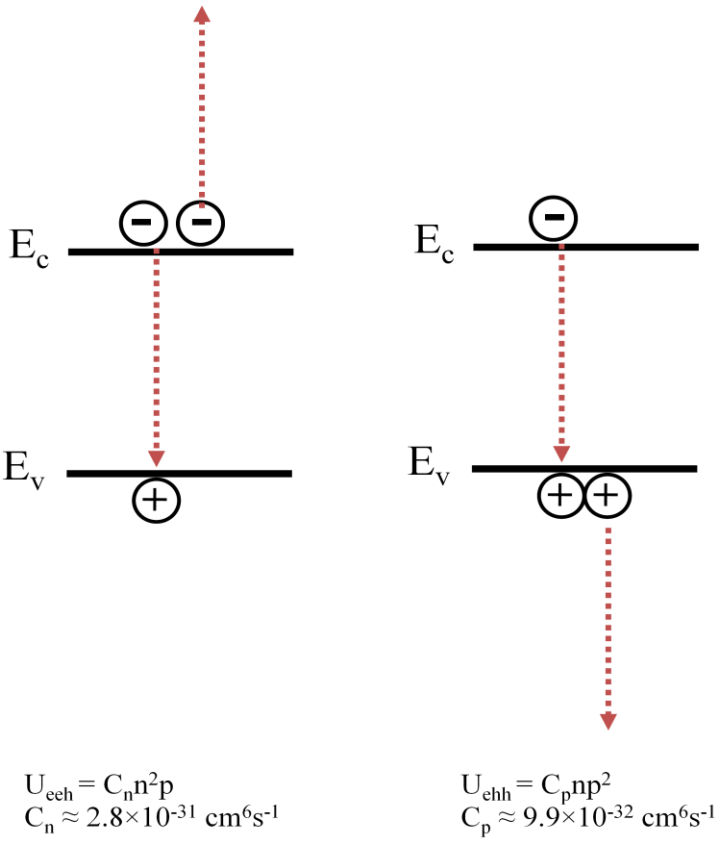



**Figure 2.12 Schematic illustration of Auger recombination.**

The total Auger recombination rate, $U_{Auger}$, is the sum of the two aforementioned processes:

$$U_{Auger} = U_{eeh} + U_{ehh} = C_n n^2 p + C_p n p^2 \qquad (2.31)$$

where $C_n$ and $C_p$ are electron and hole auger coefficients [23]. The Auger lifetime in heavily doped n-type and p-type silicon materials under low and high level injections are given by:

For n-type Si, $$\tau_{Auger,LLI} = \frac{1}{C_n N_D^2} \text{ and } \tau_{Auger,HLI} = \frac{1}{(C_n + C_p)\Delta n^2} \qquad (2.32)$$

For p-type Si, $$\tau_{Auger,LLI} = \frac{1}{C_n N_A^2} \text{ and } \tau_{Auger,HLI} = \frac{1}{(C_n + C_p)\Delta n^2} \qquad (2.33)$$

Therefore, Auger recombination is the dominant mechanism in heavily doped emitter regions or at high level injection under concentrated sunlight.

**Shockley-Read-Hall (SRH) recombination** is referred to the recombination associated with the defect levels present in the bandgap due to impurities or crystal imperfections (Figure 2.13). It was first analyzed by Shockley, and Read and Hall and therefore this process is named SRH recombination theory [16, 24].

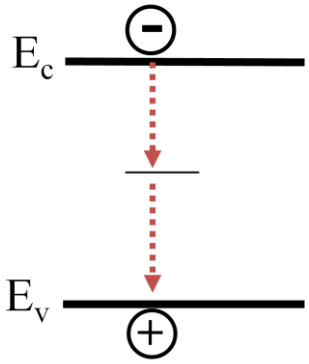



**Figure 2.13 Schematic illustration of Shockley-Read-Hall Recombination.**

The recombination rate, $U_{SRH}$, for a single defect level is given by

$$U_{SRH} = \frac{np - n_i^2}{\tau_{p0}(n + n_1) + \tau_{n0}(p + p_1)} \tag{2.34}$$

$\sigma_n$ and $\sigma_p$ are electron and hole capture cross sections, $v_{th}$ is the thermal velocity, and where

$$\tau_{n0} \equiv \frac{1}{\sigma_n v_{th} N_t} \quad \text{and} \quad \tau_{p0} \equiv \frac{1}{\sigma_p v_{th} N_t} \tag{2.35}$$

$n_1$ and $p_1$ are the electron and hole concentrations where Femi level $E_F = E_t$.

$$n_1 \equiv n_i \exp\left(\frac{E_t - E_i}{kT}\right) \quad \text{and} \quad p_1 \equiv n_i \exp\left(\frac{E_i - E_t}{kT}\right) \tag{2.36}$$

where $n_i$ is the intrinsic concentration, $E_i$ is the intrinsic energy level, T is the temperature and k is the Boltzman constant.

From the above equation, the SRH recombination lifetime can be obtained as:

$$\tau_{SRH} = \frac{\tau_{no}(p + p_1) + \tau_{po}(n + n_1)}{n_0 + p_0 + \Delta n} \tag{2.37}$$

The SRH recombination lifetime under low and high injection are given as follows:

For n-type Si, $\tau_{SRH,LLI} = \tau_{po} + \frac{\tau_{no}(\Delta n + p_1)}{N_D}$ and $\tau_{SRH,HLI} = \tau_{po} + \tau_{no}$ (2.38)

For p-type Si, $\tau_{SRH,LLI} = \tau_{no} + \frac{\tau_{po}(\Delta n + n_1)}{N_A}$ and $\tau_{SRH,HLI} = \tau_{po} + \tau_{no}$ (2.39)

For deep or midgap traps under low level injection:

For n-type Si, $\tau_{SRH,LLI} = \tau_{po}$ (2.40)

For p-type Si, $\tau_{SRH,LLI} = \tau_{no}$ (2.41)

Deep traps are the most effective recombination centers and have adverse effects on the solar cell performance.

***Surface recombination*** is associated with the defect levels within the bandgap at the surface due to abrupt termination of the crystal lattice material (Figure 2.14). These surface states promote recombination which can be analyzed by applying the bulk SRH recombination theory with minor reformations [21].

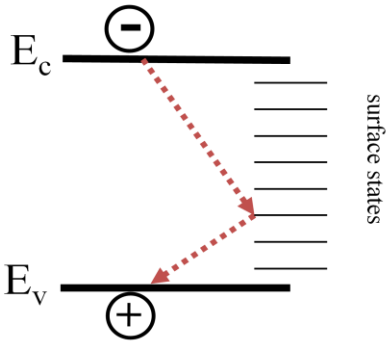



**Figure 2.14 Schematic illustration of surface recombination.**

For a single level surface state, the surface recombination rate, $U_s$, is given by:

$$U_s = \frac{n_s p_s - n_i^2}{\frac{n_s + n_1}{S_{p0}} + \frac{p_s + p_1}{S_{n0}}} \tag{2.42}$$

where $n_s$ and $p_s$ are the electron and hole concentrations at the surface, and $S_{p0}$ and $S_{n0}$ are surface recombination velocities of holes and electrons which are related to surface state density ($N_{st}$), and the capture cross-sections of the electron and hole ($\delta_n$ and $\delta_p$):

$$S_{n0} \equiv \delta_n v_{th} N_{st} \text{ and } S_{p0} \equiv \delta_p v_{th} N_{st} \tag{2.43}$$

the surface recombination velocity is related to the surface recombination rate according to :

$$S \equiv \frac{U_s}{\Delta n} = \frac{n_{s0} + p_{s0+\Delta n}}{\frac{n_s + n_1}{S_{p0}} + \frac{p_s + p_1}{S_{n0}}} \tag{2.44}$$

Surface recombination lifetime ($\tau_{surface}$) can be defined as:

$$\tau_{surface} = \left(\frac{2S}{W} + \frac{1}{D}\left(\frac{W}{\pi}\right)^2\right)^{-1} \tag{2.45}$$

where W is wafer thickness and D is the diffusion coefficient of minority carrier. For a silicon solar cell, the wafer thickness is typically around 200 μm. The second term in Equation (2.45) is very small and therefore it can be dropped resulting in:

$$\tau_{surface} = \left(\frac{2S}{W}\right)^{-1} \tag{2.46}$$

In practice, the surface states are not localized at a single energy level but are continuously distributed throughout the bandgap of a semiconductor. Moreover, the density of surface states and the capture cross-sections are dependent on their energy level. Hence, the total surface recombination rate of a real semiconductor is obtained by integrating Equation (2.42) over the entire energy bandgap [21]:

$$U_s = \int_{E_v}^{E_c} \frac{n_s p_s - n_i^2}{\frac{n_s + n_1(E)}{\delta_p(E)} + \frac{p_s + p_1(E)}{\delta_n(E)}} v_{th} \cdot D_{it}(E) dE \tag{2.47}$$

where $E_c$ is the minimum conduction band energy, $E_v$ is the maximum valance band energy, $D_{it}$ is the density of surface states per unit energy ($cm^{-2}eV^{-1}$).

Surface recombination loss has become increasingly important in industrial solar cells due to the trend toward large-area and thinner silicon wafers. Consequently, the reduction of surface recombination is an important task in this research to obtain high-efficiency commercial scale solar cells. In practice, surface recombination can be reduced by chemical passivation and field-effect passivation (Figure 2.15).

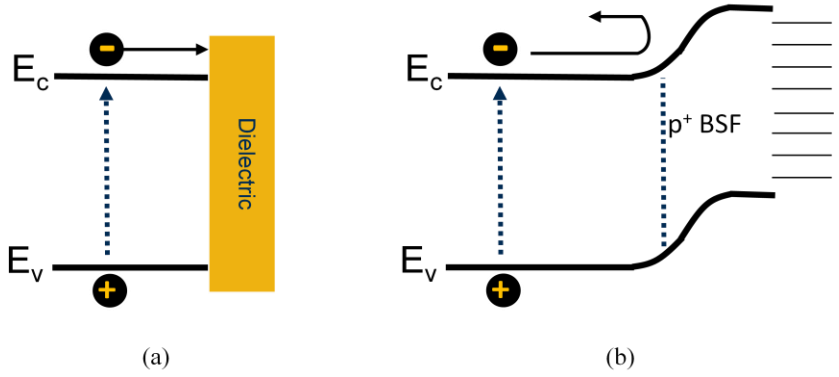



**Figure 2.15 (a) chemical passivation; (b) field-effect passivaiotn.**

The chemical passivation is based on the reduction of the density of surface states ($D_{it}$). The surface defect density can be significantly reduced by depositing thin dielectrics that can satisfy the dangling bonds at the surface of wafers. A high quality thermal oxide film ($SiO_2$) on Si is commonly used to reduce the density of surface states ($D_{it}$) and a subsequent anneal in a forming gas can further reduce the $D_{it}$ value to as low as $10^9$ $cm^{-2}eV^{-1}$ [25].

As shown in Equation (2.44), the surface recombination relates to the electron and hole concentrations at the surface. The highest recombination rate occurs when the electron and hole concentrations at the surface are equal. The field-effect passivation is based on the reduction of the electron or hole concentration at the semiconductor surface by using a built-in electric field that can repeal either the electron or the hole from the

surface. The built-in electric field can be achieved by doping the surface or by the introducing a charged dielectric at the surface. For conventional p-type cells, the field-effect passivation is typically obtained by a $p^+$-doping at the back surface called the back surface field (BSF). A negatively charged dielectric like $Al_2O_3$ can also accomplish the same by field-effect passivation.

Best strategy to reduce surface recombination is by a combination of field-effect passivation and chemical passivation. For example, thermal oxide is very effective in reducing $D_{it}$ by satisfying the dangling bonds, but it also has a positive charge density (~$10^{11}$ $cm^{-2}$) to form the field-effect passivation. However, applying positive changed dielectrics on a p-type cell needs to be carefully designed to avoid the parasitic shunting issue [26], which can arise if the p-substrate gets inverted.

The four aforementioned recombination mechanisms occur simultaneously in a semiconductor material. The effective recombination rate, $U_{eff}$, is the sum of the individual recombination rate:

$$U_{eff} = U_{rad} + U_{Auger} + U_{SRH} + U_{surface} \tag{2.48}$$

The effective lifetime is therefore given as:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{rad}} + \frac{1}{\tau_{Auger}} + \frac{1}{\tau_{SRH}} + \frac{1}{\tau_{surface}} \tag{2.49}$$

## 2.4 Summary

Solar cell is an optoelectronic device. The key to achieving high efficiency cells is to reduce optical and electrical losses in a cell. Therefore, this chapter reviewed the fundamental physics and the current understanding of the key electrical and optical loss mechanisms in solar cells. A major focus of this research is to reduce these losses through fundamental and applied research and demonstrate its success by fabricating a large-area commercial ready cell with much higher efficiency then the traditional Si cells. In typical

Si solar cells, front reflectance, gridline shading, and rear surface absorption are the major optical loss mechanisms while the SRH recombination, emitter Auger recombination, surface recombination, and resistance are the major electrical loss mechanisms. In the next chapter, high efficiency cell concepts with efficiency approaching 25% in the literature are reviewed. The goal is to identify advanced design features that can be implanted in cost effective manner. In Chapter 4, a high-efficiency large-area full Al-BSF cell is fabricated and analyzed in order to quantify these loss mechanisms and their impact of cell efficiency. This will serve as the basis for understanding and development high-efficiency low-cost advanced solar cells in the rest of the thesis work.

# CHAPTER 3

# REVIEW OF HIGH EFFICIENCY SILICON SOLAR CELLS AND LOW-COST TECHNOLOGIES

## 3.1 Introduction

In the previous chapter, efficiency loss mechanisms in a typical solar cell are reviewed. These efficiency losses must be reduced in order to obtain higher efficiency. Various types of Si solar cells have been proposed in the literature to overcome the efficiency losses. Three of the highest efficiency Si cell concepts with efficiency approaching 25% in the literature include the interdigitated back contact (IBC) cell, the heterojunction with intrinsic thin-layer (HIT) cell, and the passivated emitter and rear locally diffused (PERL) cell. This chapter begins with the review of the advanced design features in these three cells. The focus of this research is to develop low-cost high-efficiency PERC/PERL-type cells using feasible technologies, emphasis will be placed on identifying advanced design features that can be implanted in a cost effective manner.

The IBC and HIT cells provide 4-5% efficient improvement over the standard industrial Al-BSF cells because of unique design features and technologies. However, these two types of cells use complex cell structures and fabrication process along with more cost expensive n-type Si wafers. Therefore, their manufacturing cost is ~40% higher than the standard industrial cells. This does not meet our criteria of low-cost. Therefore, we will put more emphasis on PERC/PERL-type cells. The key technology differences among these advanced solar cells and the standard industrial cells will also be discussed in this section. The current state-of-the-art in this research area will be discussed. In the following section, industrially feasible technologies rather than

expensive laboratory technologies will be reviewed in order to realize cost effective high-efficiency Si solar cells in this research work.

## 3.2 Review of Three High Efficiency Silicon Solar Cell Structures with Efficiency Approaching 25%

This section reviews three high-efficiency silicon solar cells (IBC, HIT and PERL) that have achieved 23-25% efficiency in laboratory or in the production.

### 3.1.1 Interdigitated Back Contact (IBC) Cell

Figure 3.1 shows the structure of the interdigitated back contact (IBC) cell, which is also called back-contact back-junction cell. The IBC cell has interdigitated n- and p-contacts on the back side of the cell. This unique cell structure and contact scheme not only eliminates shading loss but also eliminates very high metal-silicon contact recombination at the front surface. The back contact scheme maximizes the light transmission into the cell which was originally designed for concentrator applications by the Stanford University, which achieved an efficiency of 27.5 % at 500 suns [27]. However, the manufacturing process involved multiple high-temperature diffusion and oxidation steps to form the interdigitated n- and p-regions and point contacts, and multiple photolithographic processes to isolate the back contacts. Thus, the process sequence was too expensive and time-consuming to be applicable for mass production. Over the years, SunPower has made several process modifications to reduce the manufacturing cost and increased the efficiency of one-sun IBC silicon solar cells from about 21 to 24.2% [28, 29]. This is the most efficient silicon solar cell in productions to date but it is still quite expensive relative to traditional production cell.

In addition to the back contact design, the IBC cell has several other unique features that minimize the optical and electrical losses. For instance, the IBC cells use

lightly doped front surface field in conjunction with an excellent $SiO_2$ passivation layer to reduce the front and back surface recombination velocity. In addition, the $SiO_2$ layer capped with a high refractive index metal on the back surface forms an excellent back surface reflector for long-wavelength photons. The IBC cell requires high bulk lifetime and, therefore, uses n-type Cz Si substrate with minority carrier lifetime in excess of one millisecond. The other advantages of using n-type material include higher tolerance to common impurities and defects and no light induced degradation in lifetime and efficiency, which is attributed to the formation of boron-oxygen complexes under light exposure. It is important to note that we will try to implement some of the high efficiency features of IBC, such as $SiO_2$ passivation and back surface reflector, in our low-cost cell design.

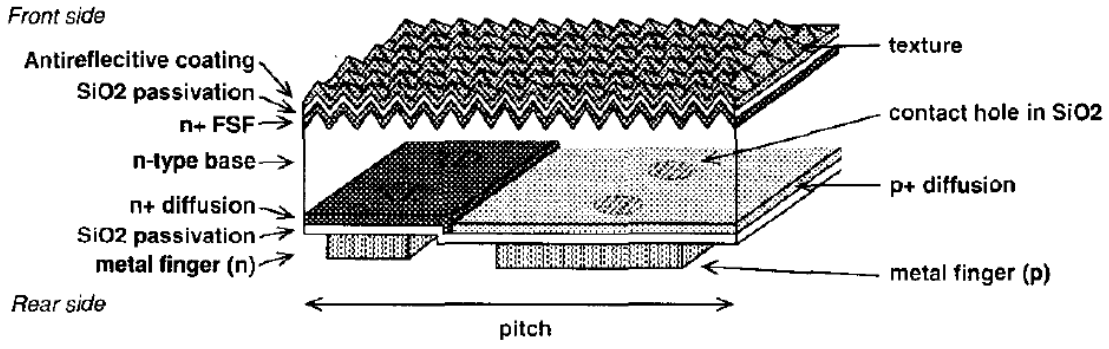



**Figure 3.1 Schematic diagram of SunPowr interdigitated back contact solar cell [30].**

### 3.1.2 Heterojunction with Intrinsic Thin-layer (HIT) Cell

Figure 3.2 shows the record high efficiency cell structure of the heterojunction with intrinsic thin-layer (HIT) developed by Sanyo Electric Co., Ltd [30]. The key features of the HIT cell are thin amorphous n- and p-doped layers (a-Si:H) for heterojunction with a very thin intrinsic amorphous layer (i-Si:H) between doped a-Si and crystalline substrate to provide excellent surface passivation. The HIT cell also uses

n-type Cz Si substrate. The a-Si:H layers are deposited at low temperature (< 300 °C). Front of the cell has transparent conductive oxide (TCO) as ARC that also reduces the sheet resistance on the front a-Si:H layer. The HIT cells generally give very high open-circuit voltage because of the large bandgap discontinuity (a-Si/c-Si) induced surface passivation. In addition, the front and rear surfaces are passivated by the i-Si:H layers which add to the excellent surface passivation. The best conversion efficiency in production for the HIT cell is 23.9% with a very high open-circuit voltage of 7483 mV on 98 µm thick n-type wafer [31, 32]. In contrast to the high $V_{oc}$, the HIT cell has a modest short-circuit current due to the absorption of photons in the front a-Si:H layer. This reduces the photocurrent collection and results in relatively lower blue response. Therefore, the challenge for this cell structure lies in balance of high voltage and the short wavelength response while maintain high fill factor. More recently 24.7% efficiency has been announcement for HIT cell by Panasonic Corporation [33].

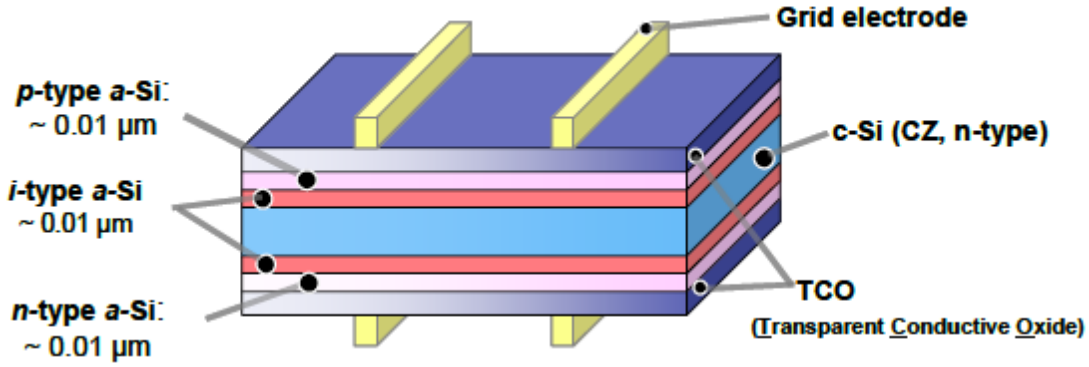
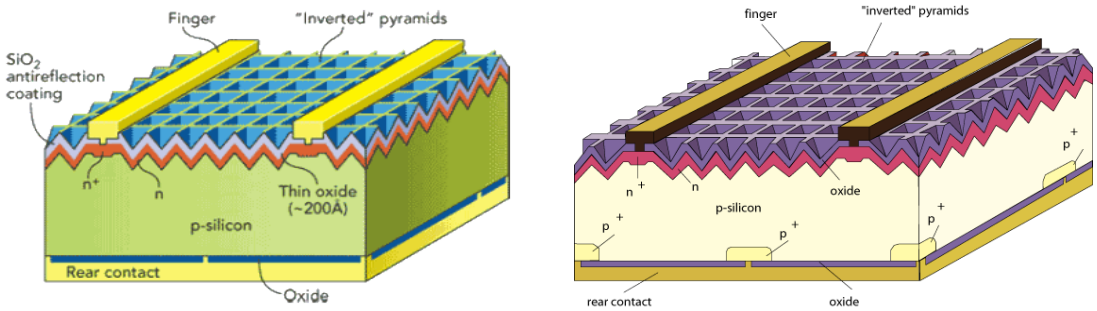



**Figure 3.2 Schematic diagram of Sanyo heterojunction with intrinsic thin layer solar cell [31].**

### 3.1.3 Passivated Emitter and Rear Cell (PERC) and Passivated Emitter with Rear Locally Diffused (PERL) Cell

The passivated emitter and rear cell (PERC) and passivated emitter with locally diffused (PERL) cell were developed in laboratory to overcome the shortcomings of the industrial full-area Al-BSF cells. The laboratory PERC solar cells achieved efficiency of 22.8% [34] while the PERL cell achieved a world record efficiency of 25% [35, 36]. The excellent cell performances were demonstrated on small-area (4 $cm^2$) p-type float zone (FZ) silicon substrate with lifetime exceeding several milliseconds. The PERC and PERL cell feature many advanced technologies to minimize the optical, recombination, and resistive losses as shown in Figure 3.3. Some of these features will be implanted in our cell design in a cost effective manner.




(a) (b)

**Figure 3.3 Schematic diagrams of (a) passivated emitter and rear cell (PERC) [34] and (b) passivated emitter with rear locally diffused (PERL) [36].**

**Error! Reference source not found.** summaries the key advanced design features which reduce optical and electrical losses in PERC/PERL silicon solar cells. Photolithography defined inverted pyramids on the front surface in conjunction with a double-layer ARC ($ZnS/MgF_2$) minimizes the front surface reflection loss. Planarized back surface and a reflector (dielectric/metal stack) on the back of the cell enhance the absorption of long-wavelength photons. Photolithography defined fine gridlines reduce

the shading loss. Both the front and rear surfaces are well passivated by thermally grown $SiO_2$ layer to minimize the surface recombination velocity. Lightly doped emitter with the front surface $SiO_2$ passivation minimizes the emitter and surface recombination losses. Heavily doped emitter underneath the gridlines reduces the metal induced recombination. Local back contacts are made through the openings in the $SiO_2$ layer to reduce back surface recombination. The back contacts are defined by photolithography to reduce the recombination of the local contacts. PERC cell has no diffusion on the back but the PERL cell is locally diffused.

**Table 3.1 Advanced design features in high-efficiency PERC/PERL cells to reduce loss mechanisms.**

| |
|---|
| **Features for optical loss reduction** |
| • Front inverted pyramids to reduce reflection loss at the front surface |
| • Double-layer ARC to reduce reflection loss at the front surface |
| • Planarized back surface to enhance back surface reflectance |
| • Back surface reflector (dielectric/metal layer) to enhance back surface reflectance |
| • Fine gridline to minimize shading loss |
| **Futures for recombination loss reduction** |
| • Lightly diffused emitter with surface passivation to reduce emitter and surface recombination losses |
| • Heavily doped at the front surface beneath the metal contact to minimize carrier recombination at metal/silicon interface |
| • Locally back surface field to minimize carrier recombination at metal/silicon contact |
| • Good surface passivation to minimize surface recombination |
| **Feature for resistive loss reduction** |
| • Selective emitter to reduce contact resistance of front contact with silicon interface |
| • Elaborate metallization schemes (Ti/Pt/Ag) to minimize contact resistances |

The PERC and PERL cells were developed to explore the optimum performance of the silicon solar cells without considering the manufacturing cost. However, eight high temperature steps, five photolithography masks, and expensive FZ Si material are not compatible with commercial production. Therefore, a photolithography free and single high-temperature process sequence will be developed in this research for reducing the manufacturing cost while maintaining several high efficiency design features of PERC and PERL cells. Recently many research groups and cell manufacturers are attempted to mass produce such structures [37-46]. The cell design will be similar to PERC cell with locally diffused BSF. Table 3.2 shows a list of the best large-area commercial PERC solar cells fabricated using various process techniques. To date, ISFH and Schott Solar are the only two institutes produced > 21% commercial PERC cells on 239 $cm^2$ Cz Si wafers. ISFH demonstrated that 46 μm fine-line dual printing process in conjunction with 5 busbar design could significantly reduce shadow losses and boost efficiency. ISFH also showed that the use of an improved aluminium (A1) paste together with an optimized rear contact geometry with narrower contact lines can raise the efficiency up to 21.2%. Schott Solar demonstrated the use of APCVD equipment to apply a rear side aluminum oxide passivation layer and employed electroplated NiCu front contacts to achieve the 21% efficient on commercial size 239 $cm^2$ p-type Cz-Si solar cell. All the other institutes fall well below the ~21% peak efficiency on the commercial PERC cells. These show the challenges in getting such high-efficiency (~21%) PERC cells using industrially feasible processes and equipment on commercial-grade Cz large-area (239 $cm^2$) silicon wafers. We will attempt to make ~21% efficient cells using ion implantation which reduces the number of processing steps, simple oxide passivation at no additional cost, screen printed contacts with three busbars to reduce the cost of metallization and Ag. The next section reviews the state-of-the-art PV technologies that can simplify the fabrication of PERC/PERL cells.

**Table 3.2 List of the best commercial grade large area PERC silicon solar cells fabricated using various processing techniques.**

| Institute | Material | Area ($cm^2$) | η (%) | Key Techniques | Yr./Ref. |
|---|---|---|---|---|---|
| ISFH | Cz | 239 | 21.2 | 5 busbars, 46 μm Ag gridline with double print; improved Al for rear contacts | 2014/[43] |
| Schott | Cz | 239 | 21.0 | APCVD $Al_2O_3$ rear passivation; electroplated NiCu front contacts | 2013/[44] |
| SunTech | Cz | 155 | 20.3 | $n^{++}$selective emitter; $p^{++}$ locally diffused BSF | 2012/[38] |
| Fraunhofer ISE | MCz | 239 | 20.2 | Laser doped selective emitter; LFC; thermal $SiO_2/SiN_x$ rear passivation | 2013/[45] |
| Q-cell | Cz | 239 | 20.2 | Laser-fired contacts | 2011/[37] |
| Canadian Solar | Cz | 239 | 20.1 | Ion implanted emitter; $Al_2O_3/SiN_x$ back passivation | 2014/[46] |

## 3.2 Review of Industrially Feasible Low-Cost Technologies for Producing High-Efficiency PERC Cells

Since the cell structure proposed in this thesis is similar to PERC, in this section, industrially feasible solar cell technologies that can be adopted for low-cost PERC cells are discussed. Some of these will be implanted to fabricate commercial grade PERC cells in this research.

### 3.2.1 Low-Cost Selective Emitter Technologies

Standard industrial silicon solar cells typically uses a homogeneous emitter with sheet resistance in the range of 50 to 70 Ω/sq to attain high phosphorous surface concentrations necessary for low contact resistance between the silicon and the low-cost screen-printed front metal contacts. However, the highly doped emitter leads to several undesirable effects including a poor short wavelength response and a high emitter saturation current density due to high Auger recombination and bandgap narrowing within the heavily-doped emitter. These loss mechanisms reduce both the short-circuit current density ($J_{sc}$) and open-circuit voltage ($V_{oc}$) of the cell. Therefore, the compromise has to be made between resistive and recombination losses in conventional $POCl_3$-diffused homogeneous emitter cells. However, PERC cell design showed that solar cell performance can be improved appreciably by a selective emitter technology which involves highly doped region under the grid for good contacts but lightly doped region in the field for lower $J_{oe}$ (Figure 3.4). As a result, a higher $J_{sc}$ is achieved due to a better blue response and a higher $V_{oc}$ is achieved due to lower $J_{oe}$, without compromising the contact quality.

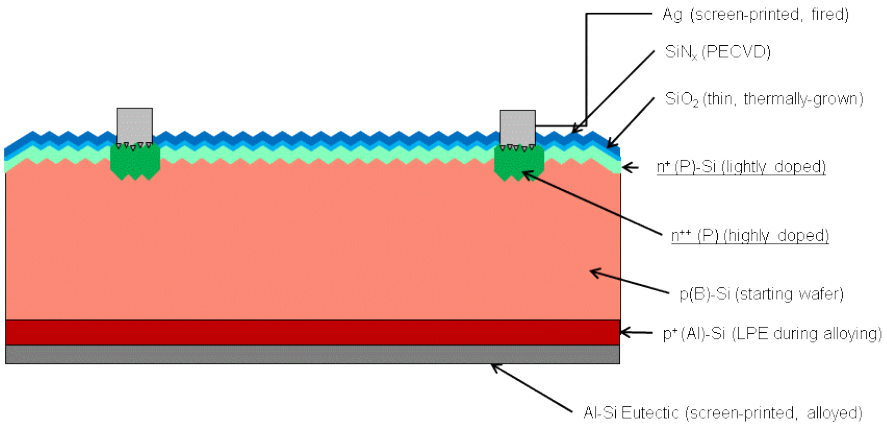



**Figure 3.4 Selective emitter solar cell.**

In the original PERC cell, the selective emitter was accomplished by photolithography which is not acceptable for mass production. Recently, many low-cost approaches have been attempted to make selective emitters, such as doped Si inks [47, 48], oxide diffusion mask [49], ion implantation [50], etch-back process [51], and laser doping [52-56]. A more thorough review of selective emitter can be found in the publication by Hahn [57]. Table 3.3 lists the IV parameters achieved with full-area Al-BSF cells. All the approaches showed ~0.5% improvement in cell efficiency; however, most of the approaches required few extra steps and/or a second high temperature diffusion which add to the cost and complexity in the cell fabrication. Therefore, in this thesis, a novel selective emitter formation process using ion-implantation technology was developed (in cooperation with Varian and Suniva) which eliminates additional steps [50]. Ion implantation simplifies the processing of selective emitter because it eliminates non value added steps like phosphosilicate glass (PSG) removal and laser edge-isolation. In addition, both differences can be achieved in a single high temperature step because ion implantation allows selective implantation. As a result, the total numbers of process

steps are reduced. This reduces processing cost while providing improved blue response and lower emitter saturation current density. This research addresses the importance of optimizing the implantation anneal for maximizing device performance in conjunction with the optimization of in-situ oxide thickness and surface passivation quality.

**Table 3.3 The best cell IV parameters and average efficiency for various selective technologies [57].**

| SE technology | Company/ Institute | Size [mm] | $V_{oc}$ [mV] | $J_{sc}$ [mA/cm$^2$] | FF [%] | $\eta_{max}$ [%] | $\eta_{av}$ [%] |
|---|---|---|---|---|---|---|---|
| Doped Si Ink | Innovalight | 125/156 | 637 | 37.5 | 79.0 | 18.9 | 18.6 |
| Oxide Diffusion Mask | Centrotherm | 156 | 634 | 37.2 | 79.2 | 18.7 | 18.6 |
| Ion Implantation | Varian | 156 | 643 | 37.3 | 78.4 | 18.8 | 18.5 |
| Etch-back | Univ. Konstanz | 125/156 | 640 | 37.9 | 78.4 | 19.0 | 18.5 |
| Laser Doping (P-glass) | Univ. Stuttgart | 156 | 637 | 37.0 | 78.9 | 18.6 | 18.5 |
| Laser Doping (LCP) | Fraunhofer ISE/RENA | 156 | 633 | 37.3 | 80.3 | 19.0 | NA |
| Laser Doping (P-acid) | UNSW | 156 | 639 | 37.8 | 77.8 | 18.8 | 18.5 |

### 3.2.2 Single-side Etching Process to Planarize the Back Surface

Planarized back surface is important for achieving high-efficiency PERC cells because it improves the surface passivation and back surface reflectance. As described in Chapter 2, a textured surface on the front results in oblique penetration of light into the silicon material which improves the carrier collection, increases the path length, and

enhances the probability of absorption. A pyramid-like textured surface is commonly used in the industrial productions for reducing the front surface reflection. The texturing is usually carried out by a wet chemical etching at 70-80˚C in a mixture of water, potassium hydroxide (KOH) and isopropyl alcohol (IPA). Due to the anisotropic etching exposes (111) planes resulting in randomly distributed pyramids on both sides of the silicon wafers. This textured surface increases ~1.7 times in the surface area compared to the (100) planar Si wafer. Textured surface degrades the ability of thermal $SiO_2$ passivation due to the increased surface and higher $D_{it}$ (Figure 3.5) associated with the (111) textured surface [58, 59]. Therefore, to mitigate the surface recombination loss, oxidation process is optimized in this research along with enhanced light trapping by planarizing the back and capping it with oxide/nitride stack and metal to form an effective mirror.

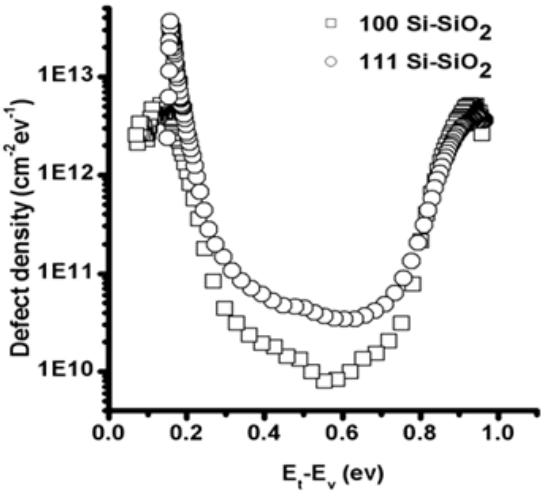



**Figure 3.5 Defect density distribution within Si forbidden bandgap. Both (100) and (111) Si structures received an FGA before metal deposition and measurement [58].**

The single-side planarization has been used in several high efficiency small-area (4 $cm^2$) FZ laboratory silicon solar cells [35, 36, 60]. A well-planarized rear surface is essential to enhance the rear surface passivation quality and the internal reflectance. This approach has demonstrated efficiency improvement over the industrial screen-printed full Al-BSF cell [39, 61]. Acid-based etching using solutions of $HNO_3$ and HF, is widely used for surface polishing of silicon wafer [62]; however the etching rate is difficult to control, resulting in a rough surface [63]. Recently, RENA and SCHMID corporations have developed inline systems that transport wafers horizontally for single side chemical etching. However, the stabilization and control of such process is challenging [64]. Therefore, in this work, KOH based wet chemical etching solutions were investigated to control back surface roughness and explore its impact on passivation quality and optical performance.

### 3.2.3 Low-Cost Surface Passivation Technologies

Surface passivation is the key to achieving high efficiency cells. Planarization helps the passivation quality but choice of dielectric and its interface quality also plays a major role in determining passivation quality or surface recombination velocity (SRV). Various dielectric layers such as thermally grown silicon dioxide ($SiO_2$), plasma-enhanced chemical vapor deposited (PECVD) $SiN_x$, and $Al_2O_3$ deposited by atomic layer deposition or PECVD are promising for mass production of solar cells. Pros and cons of these promising passivating dielectrics are reviewed.

#### 3.2.3.1 Thermally Grown Silicon Doxide

Bare silicon surface recombination velocity is greater than $10^5$ cm/s, which is 3 to 4 orders of magnitude higher than what is needed for high efficiency cells. Most of the

high-efficiency (>20%) laboratory silicon solar cells generally use thermally grown silicon oxide to reduce the front and rear surface recombination velocity (SRV). For example, very low SRV (41 cm/s) has been reported for oxide passivated 0.7 Ω-cm p-type FZ Si wafers [65]. Furthermore, evaporated Al on top the oxide and followed by ~400˚C for 20 min anneal in forming gas is shown to reduce the SRV to 20 cm/s on 1 Ω-cm P-type FZ Si wafers [66]. This is important because $SiO_2$ capped with Al on the back surface also provides an excellent reflector for the long wavelengths that can reach the back surface without getting absorbed. This can significantly improve light trapping and enhance the short-circuit current of the cell. However, high quality thermal oxides usually require high temperature oxidation (> 1000˚C) which can reduce throughput and lead to a significant degradation of bulk lifetime, particularly in the case of lower cost defective multicrystalline silicon wafers. Therefore, this research focuses on the development of low temperature and short oxidation process to achieve high quality that is comparable to Al alnealed high-temperature $SiO_2$. In addition, passivation study in this research is performed on industrial grade 239 $cm^2$ p-type CZ Si wafers that are used for mass production of silicon solar cells today.

#### 3.2.3.2 Plasma-enhanced chemical vapor deposition –$SiN_x$

Silicon nitride ($SiN_x$) grown by plasma-enhanced chemical vapor deposition is widely used as an antireflection coating as well as a surface passivation layer for the phosphorous doped emitter on p-type silicon. $SiN_x$ is also known to provide excellent passivation (SRV <10 cm/s) on p-type Si wafers [67] by inducing an inversion layer due to its high positive charge density of ~$10^{12}$ $cm^{-2}$ [26]. However, when $SiN_x$ is used for rear passivation for PERC-type solar cells, this electron-rich inversion layer shunts the local back contacts resulting significant loss in the short-circuit current density due to the out flow of electrons from the back. This phenomenon is referred to as parasitic shunting.

Therefore, direct $SiN_x$ is not a good candidate for back surface passivation. However, an appropriate stack of a thin thermal oxide capped with PECVD $SiN_x$ can provide a high quality passivation as well high internal reflectance without parasitic shunting [68]. This provided the motivation in this research to examine and optimize the formation of low-cost oxide/nitride stack to achieve high quality passivation and internal reflectance.

#### 3.2.3.3 Atomic layer deposition of $Al_2O_3$

Recently it was demonstrated that a thin $Al_2O_3$ film grown by atomic layer deposition system can also provide an excellent surface passivation on 1 Ω-cm p- and n-type Si wafers as well as on boron-doped $p^+$ emitters [69-72]. This is because, contrary to PECVD $SiN_x$ film, $Al_2O_3$ film contains very high negative charge density (~$10^{13}$ $cm^{-3}$) which forms an accumulation layer in p-Si, so no parasitic shunting occurs. This is because minority carrier electrons are repelled back into Si by the accumulation layer when $Al_2O_3$ is used for rear side passivation of p-type PERC solar cells [73]. This provides the motivation in this thesis to evaluate the passivation quality and thermal stability of $Al_2O_3/SiN_x$ stack and its impact on PERC cell performance.

### 3.2.4 Low-Cost Local Back Contact Technologies

Local rear contacts are essential for high efficiency PERC cells because it reduces the metal induced recombination and absorption of long wavelength photons in the metal. The concept of local rear contacts through dielectric passivation was introduced by Swanson [27] and Blakers [34]. However, high cost and low throughput associated with photolithography to pattern the rear passivation layer combined with evaporated aluminum layer limited the use of this concept for industrial cells. Few years ago, a simplified process laser-fired local contact (LFC) was developed at the Franhofer ISE

[74]. The LFC technology drives the metal locally through the dielectric with the help of laser to form local Al-BSF and has given > 20% efficient cells on small area 4 $cm^2$ FZ wafers with a photolithography front contact [75]. Recently, LFC process with screen-printing technology is also being investigated [76-80].

A more simplified process involving screen-printing metal dots and firing though the dielectric layer to form the local back contacts and LBSF has also been investigated [81]. However, the approach has not yet been successful because use of thicker dielectric layer for back reflector presents a barrier to fire through contacts.

Another low-cost approach to define local contacts involves screen-printing an etching paste, which contains phosphoric acid to etch through the dielectric layer. The etching of the dielectric is carried out by heating the wafers on a hot plate or in an infrared belt furnace to facilitate. Then the fried etching paste is removed in a dilute potassium hydroxide solution. This method has also given > 20% efficient Si cells on small-area 4 $cm^2$ FZ wafers [82]. However, the baking step in this approach is very sensitive to the wafer and dielectric. Non-uniform heating could lead to incomplete etching, non-uniform BSF, and parasitic shunts [83]. Above challenges with low-cost technologies for local BSF provided the motivation to explore more reliable low-cost commercial alternative for local Al BSF and contacts. The effect of process parameters, size and shapes of vias through the dielectric on cell performance is also studied. Two popular via geometries – lines and points for local back contacts are investigated and optimized by a combination of modeling and experimental validation in this thesis.

### 3.2.5 Finer Gridline Metallization

Finer gridlines are important because it increases more light to enter the cell and reduce metal induced recombination on the front. Screen-printed contacts currently dominate the photovoltaic industry because of simplicity and lower manufacturing cost.

However, the conventional screen-printing technology has some limitations for achieving ≥ 20% efficiencies. The disadvantages of screen-printing include low aspect ratio of the gridlines and the high line resistance, which limit the cell performance. In addition, screen-printing is a contact process which can easily break thin wafers, presenting a barrier to lower cost thinner cells. Some research groups have demonstrated new techniques to produce finer gridlines and higher aspect ratios to overcome the shortcomings of screen-printed cells [84-86]. However, cost effective production using these technologies still remains a challenge.

Various non-contact printing techniques have been presented in the literature [87, 88], including ink jetting and direct aerosols to form a seed layer for electro plating followed by micro-dispensing of thick films. However, these approaches require multiple processing steps to achieve the desired thickness for good contacts. In this research, a novel one-step direct printing technology is used to achieve narrow gridlines with high aspect ratios. In addition, front grid pattern design is optimized to achieve higher efficiency (> 20%) by exploiting this new technology.

## 3.3 Summary

This chapter provides a review of three high-efficiency silicon solar cell structures (IBC, HIT, and PERL) that have achieved ~25% efficiency. The IBC cell exhibits a unique back-contact back-junction design that can completely eliminate the shading loss. The HIT structure proves the excellent surface passivation quality by using a-Si layer on crystalline Si to form a heterojunction. Although the IBC cell and HIT cell allow 4-5% efficient improvement over the standard industrial Al-BSF cell, their manufacturing costs are ~40% higher than the traditional Al-BSF cells due to complexity and use of expensive n-type Si wafers. The PERC and PREL cells reveal several advanced design features which can improve optical, electrical and resistive losses simultaneously. Fabrication of

the laboratory PERL cells, however, requires several time-consuming photolithography and high-temperature steps. If low-cost commercial techniques are capable of fabricating PERC/PERL-type cells without the need for photolithography, such high efficiency solar cells would become viable candidates for mass production. This section also reviewed several low-cost technologies that can be implanted to produce PERC cells. These technologies include selective emitter formation, surface planarization, dielectric passivation, fine line metallization and local back contact formation. This research focuses on the development of low-cost industrially feasible technologies to achieve high-efficiency PERC-type cells. This objective will be achieved through five research tasks which will be described in the following chapters. In Chapter 4, commercial Al-BSF cells will be fabricated and evaluated to establish a technology roadmap for low-cost high-efficiency advanced Si solar cells. In Chapter 5, selective emitter using a novel ion implantation technology will be developed. In Chapter 6, high-efficiency rear passivated Si solar cells with local Al-BSF and screen-printed contacts will be developed. In Chapter 7, finer line direct printing technology will be developed. In Chapter 8, simplified PERC cells with low-cost homogeneous emitter will be developed. Chapter 9 will apply these developed technologies to light induced degradation free Indium doped silicon material. Chapter 10 suggests research guidelines to further improve the commercial cell designs and fabrication sequences developed in this thesis.

# CHAPTER 4

# FABRICAITON AND EVALUATION OF COMMERCIAL AL-BSF SOAR CELLS TO ESTABLISH A TECHNOLOGY ROADMAP FOR LOW-COST HIGH-EFFICIENCY ADVANCED SILICON SOLAR CELLS

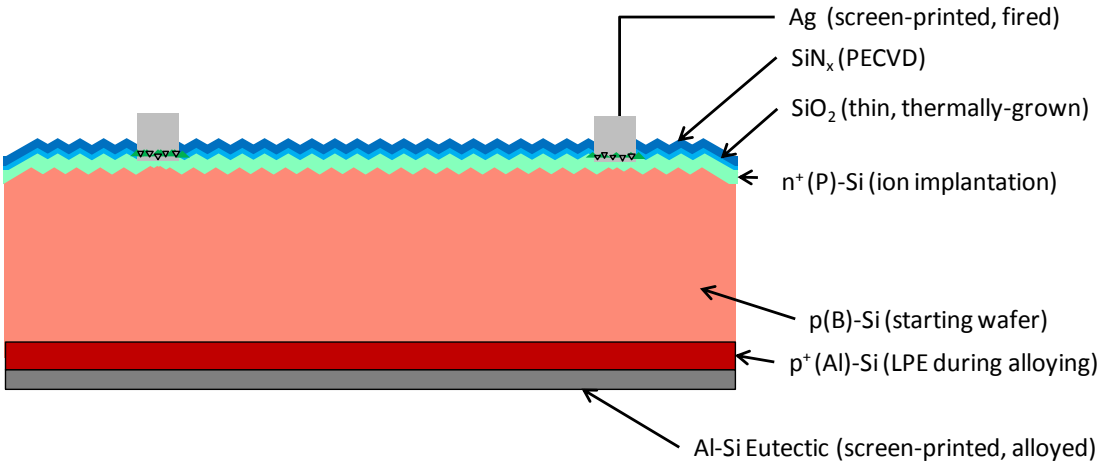
In Chapter 3, physics and operation of Si solar cells and efficiency limiting mechanisms were discussed. This chapter quantifies the losses in a typical commercial screen-printed full Al-BSF Si cell today. Therefore, the first step in this research involved fabrication of state-of-the-art 18.3% efficient production cells using screen-printing technique on large-area (239 $cm^2$) Cz Si wafers. These cells are currently about 19% efficient. Next, a methodology was developed through detail characterization and modeling to identify and quantify the loss mechanisms in these baseline cells. Then a technology roadmap was developed by extensive device modeling to establish requirements to enhance Si solar cell efficiency to about 21% using commercial ready technologies and equipments.

## 4.1 Fabrication of State-of-the-Art Screen-Printed Solar Cells with Full Al-BSF

Figure 4.1 shows the structure and the process sequence of a typical baseline commercial cell. In this task best in class production size 239 $cm^2$ Si cells with screen-printed front contact and full Al-BSF were fabricated on 180 μm thick p-type boron-doped commercial grade Cz wafers with a base resistivity of 1-3 Ω-cm. The fabrication process begins with saw damage removal in a heated KOH solution followed by alkaline texturing of both sides of the silicon wafers. After a standard clean, the wafers were

loaded in the $POCl_3$ diffusion furnace for the phosphorous–doped $n^+$ emitter formation. A diffusion temperature of 855˚C was used for 20 minutes where the phosphorous silicate glass (PSG) was deposited on the wafer surfaces. This process step was followed by an in-situ 45 minutes $N_2$ drive-in at the same temperature to obtain ~60 Ω/sq phosphorous-doped emitters. Next, the wafers were dipped in 10% HF to remove the PSG layer. An anti-reflective $SiN_x$ film was deposited on the front side using commercial PECVD equipment. Next, back Ag soldering pads was screen-printed on the rear side and then dried at 200˚C. Then Ag grid was screen-printed on the top of $SiN_x$ film, and then dried at 200˚C followed by printing Al on the exposed rear side. Next, Ag and Al contacts were co-fired in a belt furnace followed by laser edge isolation to isolate front and back sides. This simple process sequence is widely used in production today.

The light I-V data was obtained on a tester calibrated using Fraunhofer validated cells. Following the I-V measurement, the internal quantum efficiency (IQE) and front surface reflectance were measured. To determine the bulk lifetime, a completed cell was etched down to the bare Si wafer followed by standard cleaning and surface passivation with an iodine/methanol solution. Then the effective minority carrier lifetime was measured by Sinton's QSS-PC method [89]. The emitter doping profile was measured by spreading resistance profile (SRP). The junction leakage current density ($J_{o2}$) and second diode ideality factor ($n_2$) were determined by Suns-$V_{oc}$ method [90]. With the help of all the above measured input parameters, PC1D device modeling program was used to extract electrical and optical parameters by matching the measured I-V, IQE, and reflectance simultaneously [91]. This methodology involving detailed characterization and modeling leads to a very good quantitative understanding of the various loss mechanisms in the baseline cell. The required material and device parameters for high-efficiency solar cell can then be determined by extending PC1D simulation to establish the most effective and practical roadmap for raising the cell efficiency.




**Processing Sequence:**

1. Saw damage etch/texture
2. $POCl_3$ diffusion (both sides)
3. Removal of phosphosilicate glass
4. $SiN_x$ deposition on front
5. Print/dry back Ag soldering pads
6. Print/dry back Al contact
7. Print/dry front Ag gridlines
8. Co-fire
9. Laser edge isolation

**Figure 4.1 Structure and process sequence of a typical commercial cell.**

## 4.2 Results and Analysis

Figure 4.2 shows the I-V data for the best screen-printed Al-BSF cell achieved on the commercial grade 239 $cm^2$, 2.0 Ω-cm Cz Si wafers in this study. The 18.3% efficiency of the baseline cell was consistent with the industrial production when this research work started in 2009. Current baseline production cell efficiencies have reached ≥19% using $POCl_3$ diffusion. The 18.3% efficient cell was then characterized and modeled using physical device structure and characteristics to get insight into the efficiency limit of the baseline cell structure. PC1D was chosen as the device simulation tool in this research work because it is the fastest way to simulate a screen-printed silicon solar cell even though it accounts for only one-dimensional carrier transport.

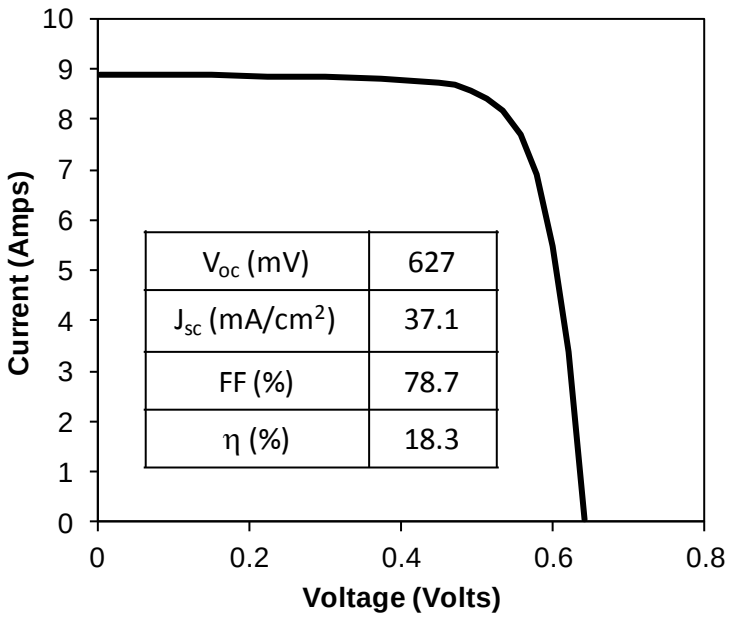



**Figure 4.2 I-V measurements for the 18.3% Al-BSF cell on commercial grade 239 cm$^2$, 2.0 Ω-cm Cz silicon.**

Table 4.1 shows the set of parameters used to describe and simulate the 18.3% efficient cell. The measured data and extracted parameters are listed along with the modeled I-V data in the same table. All the key experimentally determined parameters, such as the emitter doping profile (SRP in Figure 4.3), base doping, bulk lifetime, junction leakage current density, second diode ideality factor, and surface texture properties, were fed into to the PC1D device program to simulate the baseline cell. The front surface recombination velocity (FSRV) of 65,000 cm/s and the back surface recombination velocity (BSRV) of 400 cm/s were extracted by matching the measured IQE with the simulated IQE in the short wavelength (< 600 nm) and long wavelength range (900-1200 nm), respectively. The back surface reflectance (BSR) of 70% was extracted by matching the measured reflectance in the long wavelength range (> 1000 nm). These optical and electrical parameters of the cell were calculated by PC1D program using the extended spectral analysis of the cell IQE [92]. Figure 4.4 shows a

good match between the measured IQE/Reflectance and simulated IQE/Reflectance over the entire wavelength range. With all the above device parameters, the PC1D model predicted a cell efficiency of 18.3% with $V_{oc}$ of 626 mV, $J_{sc}$ of 37.2 mA/cm$^2$ and FF of 78.7% which agreed very well with the measured I-V values of $V_{oc}$ of 627 mV, $J_{sc}$ of 37.1 mA/cm$^2$ , FF of 78.7%, and efficiency of 18.3%.

**Table 4.1 Modeling parameters for the 18.3% commercial Al-BSF cell.**

| **Cell Parameters** | **Value** |
|---|---|
| Base Resistivity (W-cm) | 2 |
| $R_s$ ($\Omega$-cm$^2$) | 0.7 |
| $R_{sh}$ ($\Omega$-cm$^2$) | 3558 |
| $n_2$ | 3 |
| $J_{o2}$(nA/cm$^2$) | 374 |
| Emitter sheet resistance ($\Omega$/sq) | SRP (60 $\Omega$/sq) |
| Surface Conc. (cm$^{-3}$) | 5x10$^{20}$ |
| Texture angle (degrees) | 54.7 |
| Texture depth (mm) | 3.5 |
| $\tau_{bulk}$($\mu$s) | 250 |
| Grid shading (%) | 8.3% |
| BSRV (cm/s)/$J_{0b}$ (fA/cm2) | 400/660 |
| FSRV (cm/s)/$J_{0e}$ (fA/cm2) | 65,000/528 |
| $R_{back}$(%) | 70 |
| Modeled $V_{oc}$ (mV) | 626 |
| Modeled $J_{sc}$(mA/cm$^2$) | 37.2 |
| Modeled FF (%) | 78.7 |
| Modeled Efficiency (%) | 18.3 |

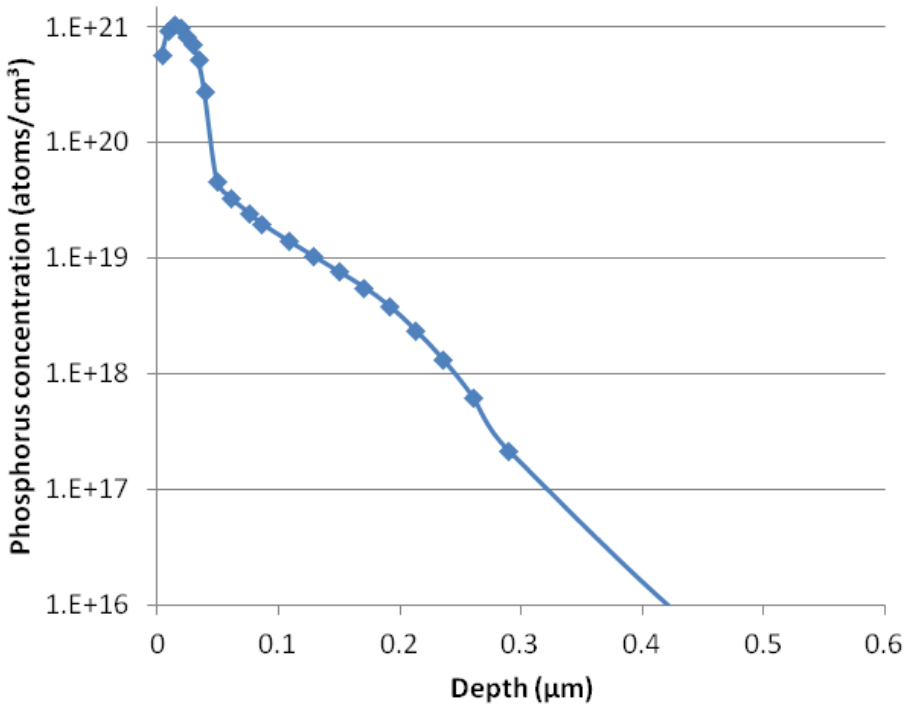



**Figure 4.3 Spreading resistance profile for the $POCl_3$ diffused emitter.**

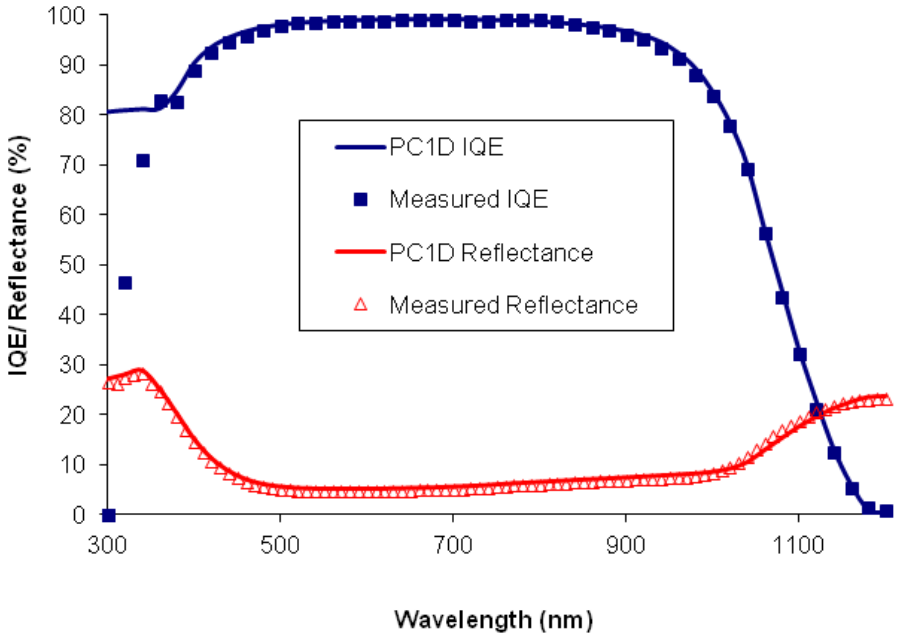



**Figure 4.4 Measured and simulated IQR and reflectance for the 18.3% Al-BSF CZ Si cell.**

Emitter and base recombination are also described by saturation current densities $J_{oe}$ and $J_{ob}$, respectively. However, $J_{oe}$ is composed of $J_{oe}$ of the metal grid lines and $J_{oe}$ of the passivated emitter between the grid lines. In order to separate and quantify the recombination loss within the emitter and the bulk of the baseline cell, the passivated emitter saturation current density ($J_{0e}$) was measured using the transient PCD method on a symmetric test structure ($n^+/n/n^+$) on an n-type ~500 Ω-cm FZ wafer [93]. The measured $J_{oe}$ of $SiN_x$-passivated textured $POCl_3$ emitter (without metal contacts) was ~396 fA/cm$^2$. The total reverse saturation current density, $J_o$, is the sum of the emitter saturation current density $J_{oe}$ and the base saturation current density $J_{ob}$ as the following equation [94]:

$$J_0 = (f)(J_{0e-met}) + (1 - f)\left(J_{0e-pass}\right) + J_{0b} \qquad (4.1)$$

where f is the fraction of the cell front surface covered with metal grid lines (8% metal coverage in this study). $J_{oe\text{-}met}$ is the $J_{0e}$ component associated with the metalized emitter surface (a representative value of 1500 fA/cm$^2$ taken from [94]), $J_{oe\text{-}pass}$ represents the passivated unmetallized emitter surface (measured to be 396 fA/cm$^2$ in this study). This gave a total $J_{oe}$ of 484 fA/cm$^2$. The total saturation current density $J_o$ value was calculated from the measured $V_{oc}$–$J_{sc}$ values using Equation (2.14), which yielded a $J_o$ value 1140 fA/cm$^2$. Subtracting the $J_{oe}$ (484 fA/cm$^2$) from $J_o$ (1140 fA/cm$^2$) gave the $J_{ob}$ value of 656 fA/cm$^2$ in this 18.3% cell. This detailed analysis reveals that the 18.3% Al-BSF cell has very high $J_{oe}$ and $J_{ob}$ values that limit the performance of the baseline cell. Consequently, we need to improve both front and rear side reduction in order to achieve ~21% efficiency.

Another approach to extract the emitter saturation current density is to use numerical device simulator PC1D. After modeling the cell (Table 4.1), the junction is forward-biased at 0.4 V in the dark to obtain the simulated minority carrier current

density ($J_p$) at the edge of the space charge region in the emitter. Then the following equation is used to calculate total $J_{oe}$:

$$J_p = J_{0e} e^{\frac{qV}{kT}} \quad (4.2)$$

where V is the applied forward-bias (0.4 V). With this numerical approach, total $J_{oe}$ was found to be 528 fA/cm$^2$. The simulated $J_{ob}$ was 660 fA/cm$^2$. There are within 10% of the measured values.

## 4.3 Technology Roadmap to Achieve 21% Efficient Manufacturable Solar Cells

After modeling the 18.3% baseline cell, various parameters of the PC1D were adjusted to find the shortest cut to 21% efficiency by establishing requirements to improve the cell efficiency via technology and cell design innovations. Figure 4.5 shows a practical technology roadmap developed in this thesis for driving the efficiency of the screen-printed CZ cells from 18.3% to 21%. Based on this roadmap, if emitter formation can be improved by using a selective emitter to reduce FSRV from 65,000 to 15,000 cm/s, while maintaining low contact resistance (FF = 78.5%), then the efficiency can increase from 18.3% to 18.8%. If the rear passivation and back contact design can be improved to obtain a back surface recombination velocity (BSRV) of 150 cm/s (as opposed to 400 cm/s) in conjunction with 93% back surface reflector (BSR), then the efficiency can rise to 19.7%. Now if the front metallization can be improved to lower the shading loss from 8.3% to 5.8%, then the efficiency can reach 20.2%. If the emitter design and front silver paste technology can be improved to contact high sheet resistance emitters (~100 Ω/sq as opposed to ~60 Ω/sq), without significant increase in contact resistance, then the homogeneous high-sheet-resistance emitter can reduce FSRV from 15,000 to 10,000 cm/s. Combining this with improved rear surface passivation (BSRV from 150 to 100 cm/s) and the back reflector (BSR from 93 to 96%), can lead to ~20.8% efficient cell. Modeling shows that at this point, if the emitter sheet resistance can be

increased to 150 Ω/sq, in conjunction with the selective emitter technology and front metal shading of ~5.5%, the FSRV can be reduced further from 10,000 to 8,000 cm/s and the cell efficiency can reach 21.1%. At this point, optical and electrical confinement of carriers is so good that the Si wafer thickness can be reduced from 180 μm to 120 μm without appreciable loss in efficiency. This is a very important benefit of this cell structure because the Si wafer accounts for ~35% of the cost of a PV module [95]. Therefore, the proposed technology roadmap not only increases cell efficiency from 18.3% to 21%, but it also leads to cost reduction if thinner cells can be manufactured.

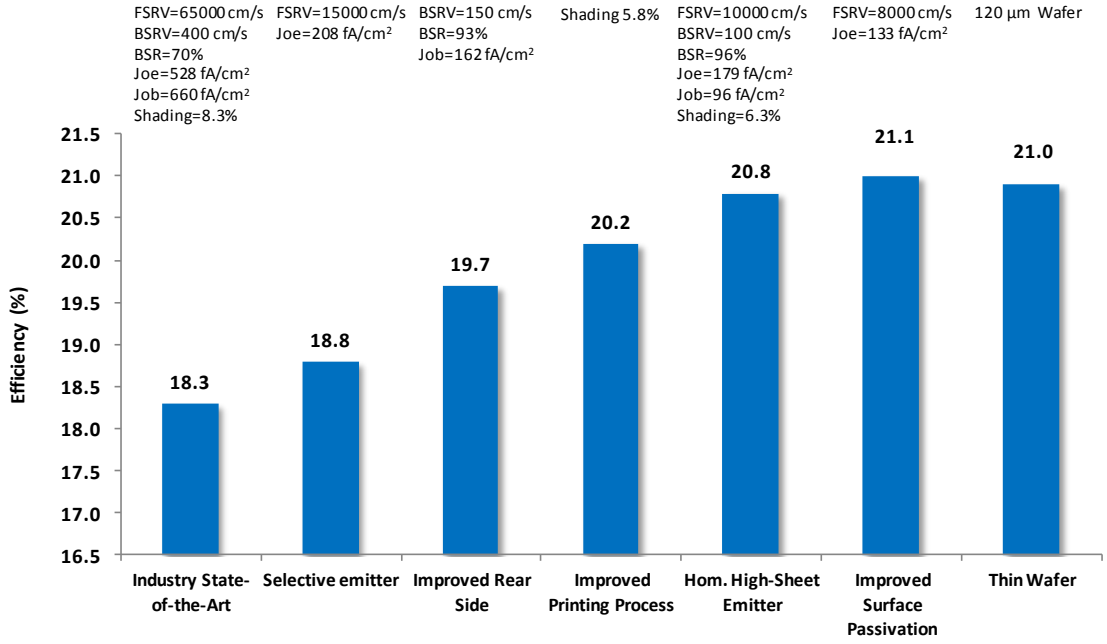



**Figure 4.5 Technology roadmap to achieve 21% efficient solar cells using a combination of industrially feasible technologies.**

In order to accomplish this challenging goal, we divided the cell development into two phases: phase-I will raise the efficiency to 20.2% and phase-II will drive to 21%. Table 4.2 summarizes the requirements and the model parameters to drive the efficiency of Cz Si cell from 18.3% to 20.2% (GEN-I PERC cell) and then to 21.1% (GEN-II PERC cell), respectively. Phase-I which will incorporate selective emitter, fine-line direct

printing technology, dielectric passivation, and enhanced optical confinement. The phase-II of the research will develop the GEN-II PERC cell, which will incorporate a low-cost homogeneous emitter, fine line screen printing and improved front and back optical confinement, in addition to all the technology innovations in GEN-I PERC cell. Specific target for GEN-II cells are:

- Optimized emitter with lower surface concentration to reduce recombination losses and enhance blue response in the emitter while maintain low contact resistance.
- Dielectric surface passivation to reduce the front and rear recombination losses (FSRV = 10,000 cm/s).
- Local rear contacts in rear passivation to reduce contact recombination losses (BSRV = 100 cm/s).
- Optimized rear reflector (BSR = 96%) to enhance optical confinement and enhance long-wavelength absorption.
- Fine line front metallization to reduce shading losses to 5.5%.

**Table 4.2 Modeling parameters for the 18.3% commercial Al-BSF cell, 20.2% GEN-I PERC cell, and 21.1% GEN-II PERC cell.**

| Cell Parameters | 18.3% Baseline Cz Cell | 20.2% GEN-I PERC Cz Cell | 21.1% GEN-II PERC Cz Cell |
|---|---|---|---|
| Wafer thickness (μm) | 180 | 180 | 180 |
| Base Resistivity (Ω-cm) | 2.0 | 2.0 | 2.0 |
| $R_{SERIES}$ (Ω-cm$^2$) | 0.7 | 0.5 | 0.6 |
| $R_{SHUNT}$ (Ω-cm$^2$) | 3558 | 23876 | 41667 |
| $n_2$ | 3.0 | 2.1 | 2.2 |
| $J_{02}$ (nA/cm$^2$) | 374 | 25 | 20 |
| Emitter sheet resistance(Ω/sq) | SRP (60 Ω/sq) | 100 | 150 |
| Junction Depth (μm) | 0.4 | 0.6 | 0.3 |
| Surface concentration (cm$^{-3}$) | $5\times10^{20}$ | $2\times10^{20}$ | $7.4\times10^{19}$ |
| Texture angle (degrees) | 54.74 | 54.74 | 54.74 |
| Texture depth (μm) | 3.535 | 3.535 | 3.535 |
| Rear surface charge (cm$^{-2}$) | Neutral | $2.2\times10^{11}$ | $2.2\times10^{11}$ |
| $t_{bulk}$ (μs) | 250 | 500 | 500 |
| BSRV (cm/s)/$J_{0b}$ (fA/cm$^2$) | 400/626 | 150/147 | 100/97 |
| FSRV (cm/s)/$J_{0e}$ (fA/cm$^2$) | 65,000/559 | 15,000/210 | 8,000/133 |
| $R_{back}$ (%) | 70 | 93 | 96 |
| Grid shading (%) | 8.3 | 5.8 | 5.5 |
| Modeled $V_{OC}$ (mV) | 626 | 658 | 670 |
| Modeled $J_{SC}$ (mA/cm$^2$) | 37.2 | 38.6 | 39.5 |
| Modeled FF (%) | 78.7 | 79.5 | 79.7 |
| Modeled Efficiency (%) | 18.3 | 20.2 | 21.1 |

## 4.4 Summary

This chapter assesses the efficiency loss mechanisms in the 18.3% efficient commercial solar cell via fabrication, detailed characterization, and PC1D device modeling program. Device modeling was extended to establish a practical roadmap that can attain ~21% efficiency. All the necessary material and device parameters were quantified to obtain the efficiency target. Detailed analysis of the baseline cell indicated that we need to reduce FSRV from 65,000 to 15,000 cm/s, BSRV from 400 to 150 cm/s, BSR from 70% to 93%, and shading loss from 8.3% to 5.8% in order to raise the 18.3% efficiency to 20.2% in phase-I. These requirements can be achieved by technology development and innovations related to selective emitter formation, improved dielectric passivation, back reflector, local rear contacts, and fine-line printing. Extended modeling showed that higher sheet resistance emitter in conjunction with further optimization of surface recombination, selective emitter, reflector and shading can raise the cell efficiency to 21% in phase-II of this thesis. Following chapters describe the technology developments and integration to achieve ~21% PERC cell efficiency.

# CHAPTER 5

# DEVELOPMENT OF SELECTIVE EMITTER USING A NOVEL ION IMPLANTATION TECHNOLOGY

Most cell manufacturers today use conventional $POCl_3$ diffusion for forming homogeneous $n^+$ emitter. Selective emitter, with heavy diffusion underneath the grid lines and light diffusion in the field, can boost cell efficiency by ~0.5% absolute. However, formation of selective emitter by $POCl_3$ tube diffusion adds multiple steps and increases cost which mitigates the benefit of high cell efficiency. In this work, ion implantation is successfully implemented for the first time for fabricating selective emitter for high-efficiency Si solar cells without introducing additional steps. This is because ion implantation can provide high quality single side patterned diffusion without the need for laser edge isolation, masking or phosphosilicate glass (PSG) removal steps. In this research, the ion-implants were done at Suniva Inc. using the first commercial implanter (Solian tool) for PV applications from Varian Semiconductor Equipment Associates (now a division of Applied Materials). Some implants were also done on Varian's Early Learning Tool (ELT). With this ion implanter, the heavy and lightly doped regions for selective emitter can be formed in a single implant step on one side of the wafer using an appropriate shadow mask during implantation followed by a single high temperature anneal. Therefore, compared to the widely used $POCl_3$ diffused homogeneous emitter in industry, ion implantation can provide cost-effective selective emitter for high efficiency and simultaneously eliminate the two non-value added steps, namely PSG removal and laser edge isolation.

In this chapter, five topics are covered. The first section introduces the basics of the Solion ion implanter. The second section discussed the annealing mechanism after ion implantation. The third and fourth sections describe fabrication and characterization of ion implanted emitters, and discuss passivation quality of the implanted selective emitter. The final section compares the performance of ion implanted selective emitter cells with conventional $POCl_3$ diffused emitter cells. Detailed characterization, modeling and analysis of the cells was performed to understand the loss mechanism and benefit of each technology innovation.

## 5.1 Basics of Ion Implantation

Ion implantation has been the dominant doping technique in integrated circuit industry for decades because it offers a precise means to introduce dopant impurities into the silicon substrate with superior uniformity and repeatability. Due to its ability to independently control the dopant profile, the junction depth and the carrier concentration, the ion implantation was used to form emitters in crystalline Si solar cells in the early 1980's [96-98]. A peak efficiency of 18% was demonstrated on laboratory scale small-area FZ Si cells [98]. Despite its superior performance, the ion implantation, however, did not come into the mainstream of PV manufacturing due to its low throughput and high cost. Until recently, a cost-effective ion implantation tool has been developed for manufacturing large-area (156 mm) solar cells at a production rate of ~25,000 cells/day which is comparable to the dominant diffusion furnace technique in the industry [99]. Consequently, ion implantation provides a great opportunity to attain low-cost high-efficiency Si cells.

Figure 5.1 shows the very first production tool called "Solion" developed by Varian Semiconductor Equipment Associates for mass production of ion-implanted solar cells. In this research, most ion-implants were done using this commercial tool.


**Figure 5.1 Varian Solion ion implantation system for the PV application [100].**

An ion implanter is basically a particle accelerator that produces a highly accelerated ion beam that can penetrate into a target silicon substrate. Figure 5.2 shows the schematic diagram of Varian Solion ion implanter. The Solion ion implanter consists of five main components: the ion source, the mass analyzer, the accelerator, the bean shaping and the end station where the silicon wafers are placed for implantation. The implanter introduces a dopant impurity into the silicon wafer by creating ions of impurity (e.g. boron, phosphorus and other dopants) in the ion source. The ions are then entered into the mass analyzer where it filters out unwanted ions by a dual-magnet ribbon-beam architecture based on ion mass. The desired ion beam is then accelerated to a preset energy by the accelerator. Finally, the ion beam uniformly and parallelly penetrates onto the target substrate where the end-station scans and moves the substrate vertically in one dimension.

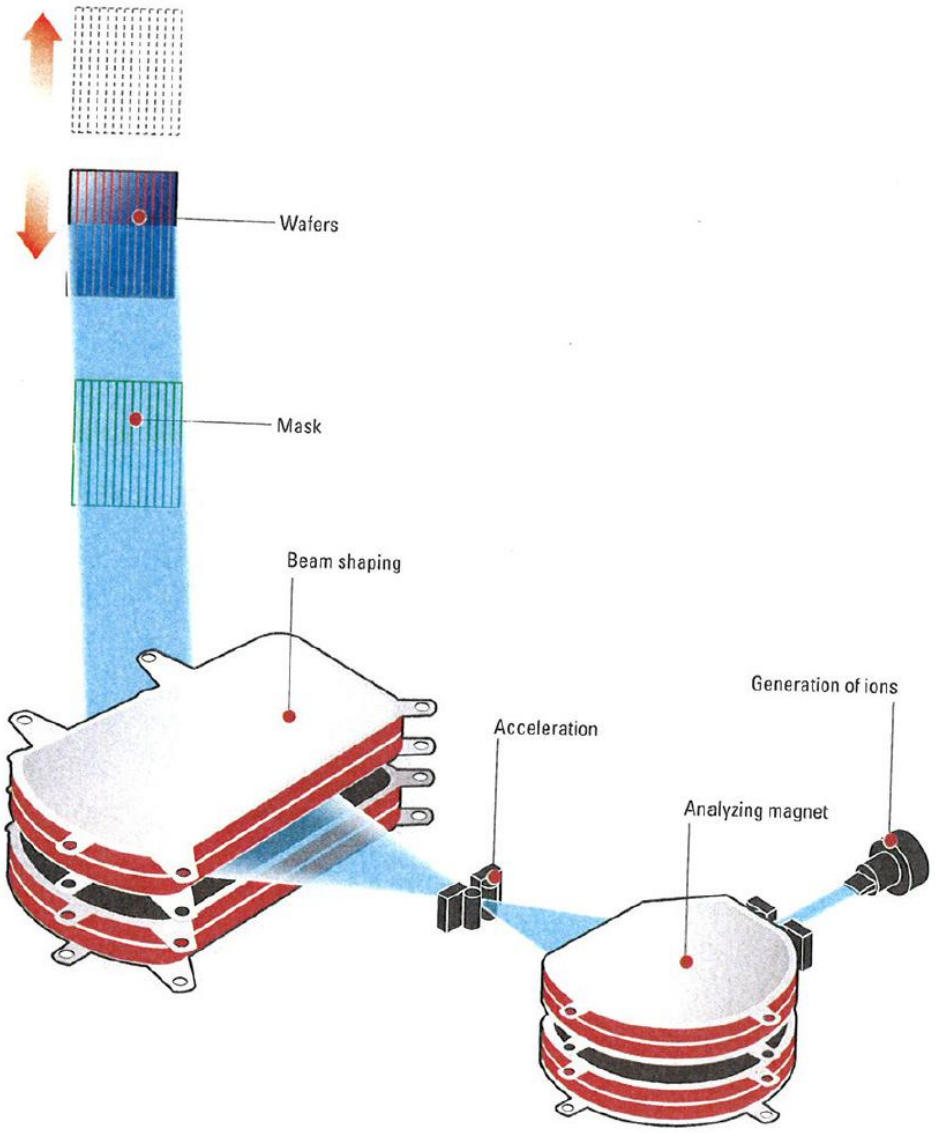



**Figure 5.2 Schematic diagram of Varian Solion ion implantation system [100].**

Development of a high quality ion implanted emitter is dependent on the design and optimization of the implanted dose, energy and angle. The dose is the total number of ion implanted ions per square centimeter. It is well controlled in the implanter by monitoring the number of atoms reaching the wafer and then cutting off the ion source when the preset level is reached. Generally, the dopant profile produced by ion

implantation can be described by a Gaussian distribution (Figure 5.3) and is expressed by:

$$N(x) = N_p \exp\left(-\frac{(x - R_p)^2}{2\Delta R_p^2}\right) \qquad (5.1)$$

where $N_p$ is the concentration at the peak of the Gaussian distribution, $R_p$ is called projection range where $N_p$ is located at the depth of $R_p$ beneath the silicon surface, and $\Delta R_p$ is called straggle which is the width of the distribution. By integrating the dopant concentration over the distribution, one can obtain the total implanted dose that yields a relationship between the peak concentration, $N_p$ ($cm^{-3}$) and the implanted dose $\phi$ ($cm^{-2}$):

$$N_p = \frac{\emptyset}{\sqrt{2\pi}\Delta R_p} \qquad (5.2)$$

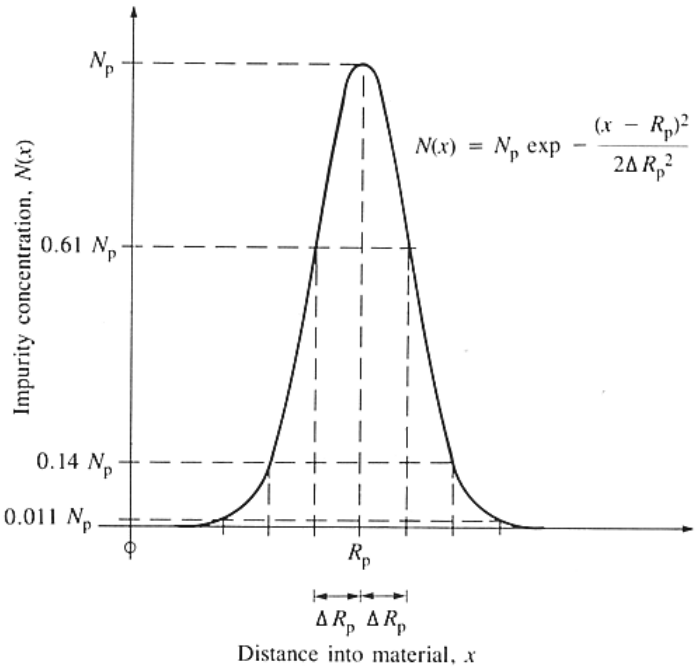



**Figure 5.3 Gaussian distribution of dopant for an ion implantation.**

In practice, the ion beam current and implantation time control the dopant concentration. For this research, the implanted does in the range of $1\times10^{15}$ $cm^{-2}$ to $7\times10^{15}$ $cm^{-2}$ was used. Note that the dose measured by the ion implantation system may not be

the same as the dose received by the silicon surface due to the textured surfaces of the solar cell. Typically the ions incident on a textured surface with an angle ~54.7˚ relative to the faces of the textured pyramids. The effective dose on the pyramid surface reduces as the cosine of the incident angle ($1/\cos 54.7^{\circ} \approx 1.73$). In other word, the implanted dose is distributed over a larger effective surface area provided by the textured surface.

The ion energy is a function of the electric field accelerating dopant atoms toward the silicon substrate. This energy is proportional to the kinetic energy of the dopant atoms. It is typically measured in the unit of electron volt (eV). The higher the ion energy, the deeper the ions are implanted into the target substrate, therefore, ion energy also controls junction depth. For this research, implant energies between 10 keV and 30 keV were used.

When ion implantation is performed on crystalline silicon, the penetration depth of the dopant can be predicted by the theory in Equation (5.1). The phenomenon called channeling can occur when the ion beam is parallel to a major crystal orientation in which ions can travel unimpeded through channels between silicon atoms in the lattice. Channeling can produce a significant tail in the dopant profile, particularly pronounced when implanting light dopants (e.g. boron) onto the substrate. To avoid this undesired effect, silicon wafers are tilted by 5 to 7 degree with respect to the perpendicular to the substrate. Another way to minimize channeling is to convert the silicon into amorphous before implantation. The other method to reduce channeling is by implant through a thin oxide to randomize the ion directions before entering the target substrate. For this study, the silicon wafer was tilted 6 degree before implantation.

## 5.2 Post Ion Implantation Annealing

The primary disadvantage of ion implantation is that the ion bombardment creates a lot of damages in the surface lattice, such that this region is no longer a perfect crystal

structure but undergoes a certain level of amorphization. In addition, the dopant atoms introduced by the implantation create silicon self-interstitials which are electrically inactive and can degrade the semiconductor properties, such as carrier mobility. These implantation-induced damages must be repaired by annealing at a high temperature. During the annealing, solid-phase epitaxy (a transition between the amorphous and crystalline phases) takes places utilizing the crystal structure of the undamaged region as a template to re-grow the surface region into a perfect crystal. Moreover, the annealing step allows the dopant atoms to diffuse into substitutional sites in the silicon lattice. The annealing temperature therefore plays a crucial role in dopant activation. The anneal time also affects the junction depth and the dopant concentration at the surface region. During the annealing, it is possible to grow a thermal oxide on the wafer to serve as surface passivation. This oxidation process also influences the diffusion behavior of the dopants. Therefore, development of a right anneal condition to form a high-quality ion implanted emitter with superior surface passivation in single high-temperature step is a major goal in this research to exploit the ability of ion implantation to achieve high performance at no additional cost. The positive impact of oxidation on cell performance and emitter quality will be discussed in Chapter 6.

## 5.3 Fabrication and Characterization of Ion Implanted Emitters

In this study, several phosphorus implanted homogeneous and selective emitters were fabricated to examine the impact of implanted dose and energy on sheet resistance, emitter profile and passivation quality. The objective of this task is to study the dose, energy and anneal conditions to optimize and establish right conditions for attaining the best selective emitter and demonstrate its high quality by emitter saturation current density $J_{oe}$ measurement, which is a measure of total recombination (bulk and surface) in

the emitter. The passivation quality of in-situ grown thermal $SiO_2$ and PECVD $SiN_x$ AR coating on an ion implanted selective emitter is studied and compared with the conventional $POCl_3$ diffused emitter.

To characterize the ion-implanted emitters fabricated in this work, 500 Ω-cm n-type FZ c-Si wafers were etched first in a heated potassium hydroxide solution (chemical formula: KOH) to remove the saw-damage, followed by alkaline pyramid texturing of both surfaces. Phosphorus ions with energy in the range of 10 to 30 keV and dose in the range of $1\times10^{15}$ to $7\times10^{15}$ P/cm$^2$ were implanted on both sides. The samples were annealed at 840˚C for 30 minutes in $O_2$ followed by 25 minutes in $N_2$ to remove the implantation damage and activate the dopants. The sheet resistance of the samples was measured using a 4-point probe, doping profiles were measured by electrochemical capacitance voltage (ECV) measurements [101] as a function of depth, and the emitter saturation current density $J_{oe}$ was measured using well established quasi-steady-state photoconductance (QSS-PC) in which carrier are excited with an appropriate light source and the rate of decay of carriers is sensed by measuring the decrease in photoconductance [93].

### 5.3.1 Sheet Resistance and Doping Profiles of Ion Implanted Emitters

The sheet resistances of the homogenous emitters formed by using different implant conditions used in this study are shown in Figure 5.4 for the 840˚C anneal for 30 minutes in $O_2$ followed by 25 minutes in $N_2$. By controlling the dose and energy combinations, the sheet resistance could be varied from 55 Ω/sq ($7\times10^{15}$ P/cm$^2$, 30keV) to 225 Ω/sq ($1\times10^{15}$ P/cm$^2$, 10keV). Clearly the sheet resistance increases with reduced implant energy and dose; moreover, the sheet resistance of the implanted emitters exhibits a very

tight distribution within a wafer as shown in Figure 5.4. These results demonstrate that ion implantation can provide great flexibility in controlling the emitter sheet resistance.

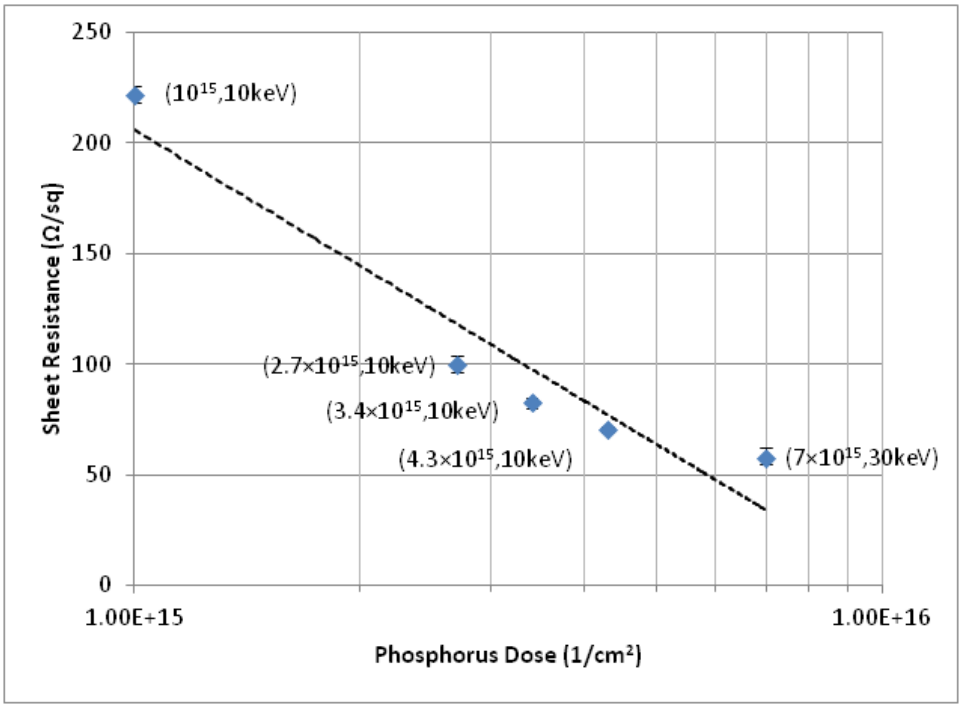



**Figure 5.4 Sheet resistances achieved through ion implantation with various phosphorus doses and energies. The samples were annealed at 840˚C for 30 minutes in $O_2$ followed by 25 minutes in $N_2$.**

ECV profiles of the phosphorus implanted emitters after the anneal are shown in Figure 5.5. For comparison, an industrial $POCl_3$ diffused 65 Ω/sq emitter is also shown on the same figure. Clear differences can be seen in phosphorus surface concentration between the industrial $POCl_3$ emitter and implanted emitters. The industrial emitter displays an electrically active P concentration of $10^{21}$ atoms/cm$^3$ for up to a depth of 0.05 μm into the wafer surface while the ion implanted emitters show almost five times smaller phosphorus concentration near surface. The high surface concentration of the industrial emitter can facilitate the formation of good quality ohmic contact between the

Si emitter and commercially available thick-film screen printed Ag pastes. However, the high doping also leads to high bulk recombination in the emitter and can also degrade the emitter surface passivation quality. To assess the impact of emitter profile and surface passivation on recombination, emitter saturation current density $J_{oe}$ for each emitter was estimated by using a Sinton WCT-120 Photoconductance Lifetime Tester. The next section will discuss the results of this study.

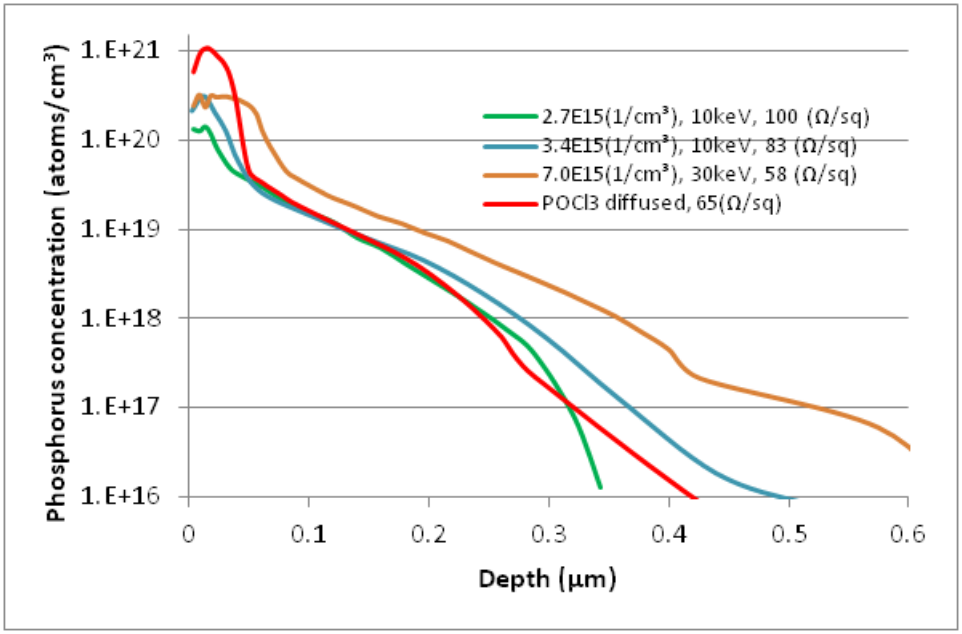



**Figure 5.5 ECV profiles of phosphorus implanted emitters and conventional POCl3 diffused emitter.**

### 5.3.2 Passivation Quality of Ion Implanted Selective Emitter

$J_{oe}$ is an excellent indicator of emitter quality. Since cell fabrication involves ion implantation, anneal, oxidation, $SiN_x$ AR coating deposition and contact firing, $J_{oe}$ was measured after each heat treatment to track the change in emitter quality and the final $J_{oe}$. Figure 5.6 shows the evolution of $J_{oe}$ of a conventional $POCl_3$ emitter and different ion implanted emitters after different cell processing steps. Figure 5.6 shows that the $J_{oe}$ of

five 55 Ω/sq to 225 Ω/sq phosphorus implanted emitters which were passivated with a ~90Å thick in-situ oxide layer grown during the implant anneal at 840˚C in oxygen ambient for 30 minute followed by a 25 minute anneal in nitrogen at the same temperature. Note that the $J_{oe}$ of all five homogeneous emitters was found to be in the range of 60-290 fA/cm$^2$ right after the 840˚C implant anneal including oxidation. However, $J_{oe}$ showed slight decreases after PECVD $SiN_x$ AR coating deposition at ~450˚C. However, after the simulated contact firing at ~750˚C for few seconds, $J_{oe}$ showed a significant reduction. The much higher $J_{oe}$ of the industrial 65 ohm/sq $POCl_3$ emitter (396 fA/cm$^2$) compared to ~100 fA/cm$^2$ $J_{oe}$ for the implanted emitters clearly shows the superiority of the Oxide/$SiN_x$ passivated implanted emitters. It is important to recognize that a low dose creates an emitter with low recombination but produces high resistive losses due to higher sheet resistance while a high dose does the opposite. To find the optimum dose and energy that will minimize emitter recombination, PC1D device modeling was used to calculate the performance enhancement from the high sheet resistance emitter using the measured profiles, sheet resistance and $J_{oe}$ numbers. It is impartment to note that PC1D is a one-dimensional model; therefore, it can only be used to model homogeneous emitters with a constant FSRV. The technology roadmap (Figure 5.7) showed that the combination of the implanted high sheet resistance emitter (~100 Ω/sq) and superior front surface passivation (FSRV = 15,000 cm/s, $J_{oe}$ ~ 100 fA/cm$^2$) can provide ~0.5% improvement in absolute efficiency. Conventional 65 Ω/sq $POCl_3$ emitter with FSRV = 65,000 cm/s, $J_{oe}$ ~ 480 fA/cm$^2$ gave a modeled efficiency of 18.3% compared to 18.8% for the oxide passivated implanted emitter. To validate this model, a selective emitter was formed with the phosphorus energy of 10 keV and dose of $2.7\times10^{15}$

P/cm$^2$ in the field region (~100 Ω/sq), in conjunction with heavily doped ~50 Ω/sq region underneath the grid line with energy of 30 keV and dose of $7\times10^{15}$ P/cm$^2$. In the next section, ion implanted selective emitter cells and conventional $POCl_3$ diffusion cells are fabricated and compared.

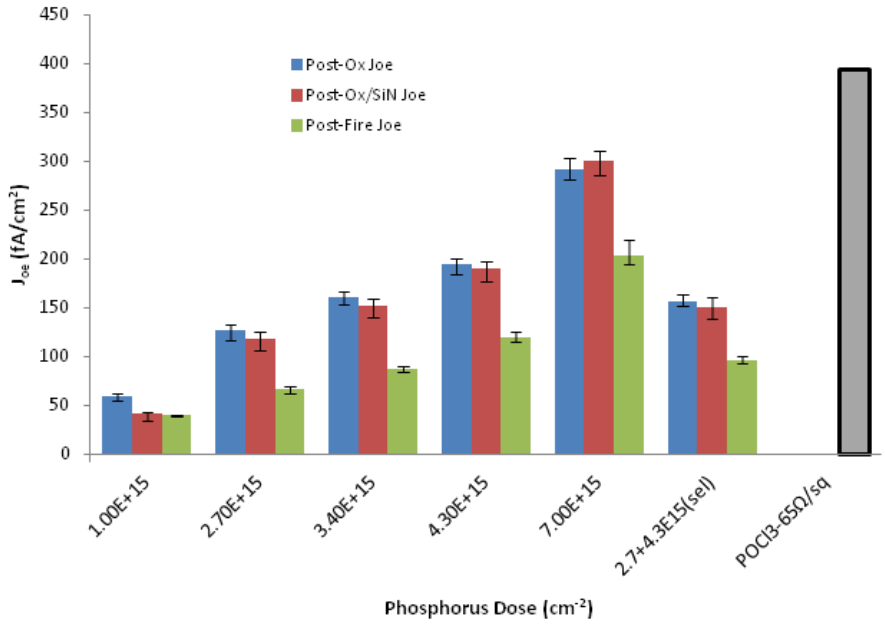



**Figure 5.6 $J_{oe}$ comparison of a conventional $POCl_3$ emitter $J_{oe}$ and different ion implanted emitters at different process steps.**

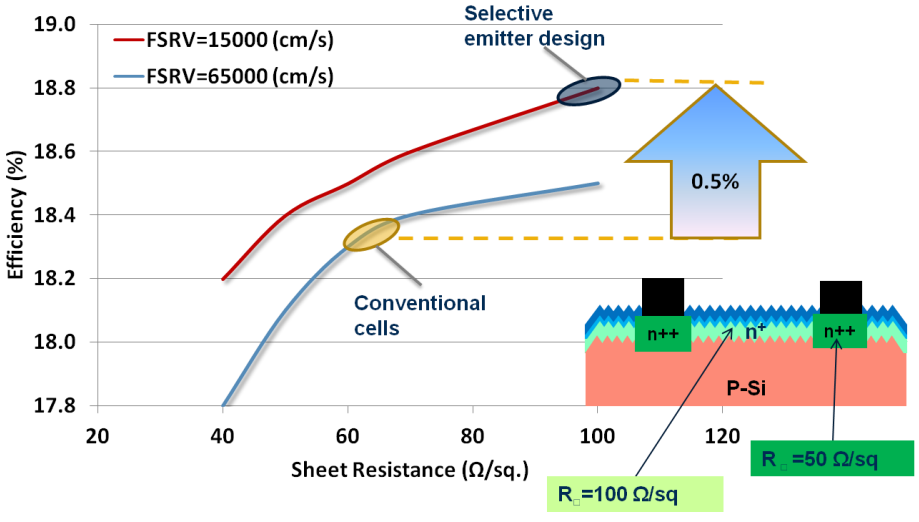



**Figure 5.7 Efficiency enhancement resulting from the high sheet resistance emitter relative to the conventional 65 Ω/sq.**

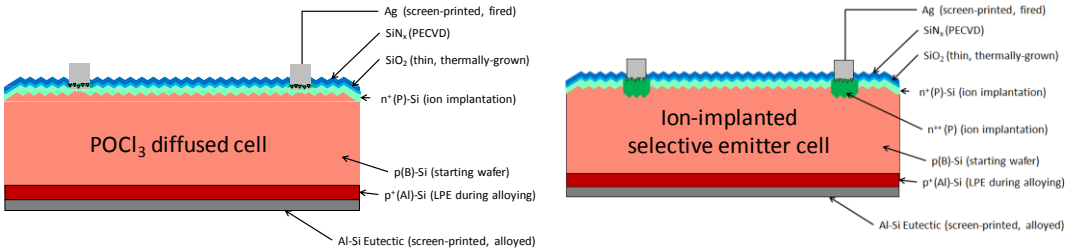
## 5.4 Experimental Demonstration of Enhanced Performance of Ion Implanted Selective Emitter Cell over the Conventional POCl3 Diffused Emitter Cell

Large-area ion-implanted selective emitter cells were fabricated on 156 mm 2 cm-Ω Cz Si wafers. The selective emitter was formed by two in-situ implants. First, the entire wafer is implanted with a lower phosphorus dose to create a 100 Ω/sq high sheet resistance field region. A proximity mask is then inserted between the wafer and the ion beam without removing the wafer, and a second implant follows. Openings in the mask define a grid-pattern of heavily doped regions to which the front screen printed contacts are aligned. The implant damage is then annealed in a tube furnace. Note that in-situ oxidation also helps in contact alignment if this alignment is carried out by pattern recognition. Because the oxide grows much faster on the heavily-doped n-type regions, the grid pattern is easily visible after oxidation. Figure 5.8 shows an optical microscope image of an ion implanted selective emitter cell. Clear contrast between the lightly doped field regions and more heavily doped contact regions can be seen for contact alignment.


**Figure 5.8 Optical microscope image of an ion implanted selective emitter cell after $SiN_x$ deposition and screen printed front contacts.**

Following the implant anneal, the wafers are sent through a standard PECVD $SiN_x$ deposition step at~450˚C. Since the passivating oxide under the $SiN_x$ contributes to

the AR effect, a thinner $SiN_x$ layer (~500 Å as opposed to 750 Å) is needed which enhances the throughput of the PECVD machine. While most selective-emitter strategies being attempted or used in production require one to four additional steps [57], the same structure is achieved with fewer processing step using our masked ion implantation approach because of the elimination of phosphorus glass removal and junction edge isolation steps (Figure 5.9).




**Processing Sequence**

1. Saw damage etch/texture
2. POCl3 diffusion (both sides)
3. Removal of phosphosilicate glass
4. SiNx deposition on front
5. Print/dry back Ag soldering pads
6. Print/dry back Al contact
7. Print/dry front Ag gridlines
8. Co-fire
9. Laser edge isolation

(a)

**Processing Sequence**

1. Saw damage etch/texture
2. Implant phosphorus on front
3. Anneal implant damage and grow thermal oxide
4. SiNx deposition on front
5. Print/dry back Ag soldering pads
6. Print/dry back Al contact
7. Print/dry front Ag gridlines
8. Co-fire

(b)

**Figure 5.9 Structures and processing sequences for (a) $POCl_3$ diffused cell and (b) ion-implanted selective emitter cell.**

Implantation energy, dose and anneal conditions were selected to achieve 100 Ω/sq (with $2.7\times10^{15}$ P/cm$^2$) sheet resistance in the field and ~50 Ω/sq (with $7\times10^{15}$ P/cm$^2$) under the grid area for the selective emitter. In-situ thin oxides were grown on the front and rear surfaces during the implant anneal and capped with appropriate thickness of $SiN_x$ coating prior to the screen-printing silver (Ag) grid on the front and back aluminum (Al) contacts. Finally both the contacts were co-fired in a belt furnace to form the grid contact on the front and a full area Al-BSF in the rear. For comparison, conventional $n^+pp^+$ solar cells were fabricated with $POCl_3$ diffused emitter, PECVD $SiN_x$ AR coating, screen-printed and co-fired front silver (Ag) and back aluminum (Al)

contacts. Figure 5.9 shows the process sequences and structures for $POCl_3$ diffused cell (a) and ion implanted selective emitter cell (b).

Table 5.1 shows the light I-V data for the ion implanted selective emitter cell and conventional $POCl_3$ diffused cell. The ion-implanted selective cell structure gave 14 mV higher $V_{oc}$, 0.3 mA/cm$^2$ higher $J_{sc}$ and 0.5 % higher efficiency compared to the traditional $POCl_3$ diffused cell. This is entirely consistent with the model calculations in Figure 5.7. Figure 5.10 shows a comparison of the internal quantum efficiency (IQE) and reflectance data of a $POCl_3$ diffused cell and an ion implanted selective emitter cell with full Al-BSF. It is clear that selective emitter cell has a superior short wavelength response compared to the $POCl_3$ diffused emitter cell. This again validates the superiority of the ion implanted emitter cell because short wavelength is mostly absorbed in the emitter region.

**Table 5.1 Light I-V data for $POCl_3$ diffused cell and ion-implanted selective emitter cell.**

| | $V_{oc}$ [mV] | $J_{sc}$ [mA/cm$^2$] | FF [%] | $\eta$ [%] |
|---|---|---|---|---|
| Selective emitter cell | 641 | 37.4 | 78.5 | 18.8 |
| $POCl_3$ Emitter cell | 627 | 37.1 | 78.7 | 18.3 |

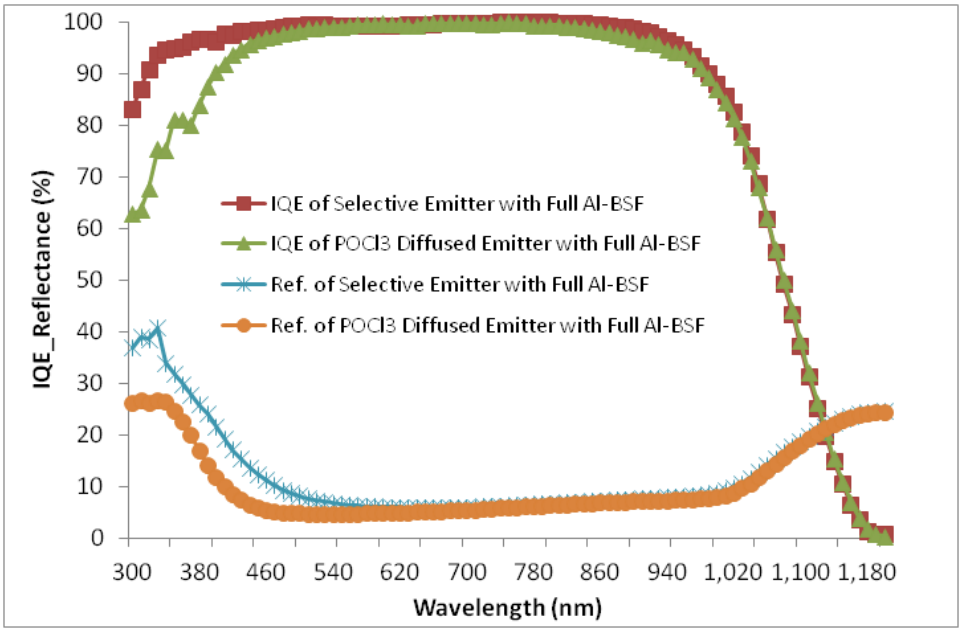



**Figure 5.10 IQE and Reflectance of $POCl_3$ emitter cell and ion-implanted selective emitter cell with full Al-BSF.**

In order to gain deeper insight into the emitter quality difference, detailed model calculations were performed to extract the emitter and base saturation current densities, $J_{oe}$ and $J_{ob}$. The modeling results are depicted in Figure 5.11 which reveals that the improvement in efficiency results from selective emitter induced decrease in FSRV from 65,000 cm/s to 15,000 cm/s. The observed improvement in $V_{oc}$ is attributed to the reduction in $J_{oe}$ from 559 fA/cm$^2$ to 162 fA/cm$^2$. The $J_{ob}$ of both the cells remains high at 626 fA/cm$^2$. Clearly, the $J_{ob}$ is much greater than the $J_{oe}$ in the selective emitter cell because the full Al-BSF gives high back surface recombination velocity of ~400 cm/s. Consequently, the efficiency enhancement from this point will involve reducing BSRV and base recombination. Roadmap established by model calculations in Chapter 4 showed that the $J_{ob}$ needs to be < 150 fA/cm$^2$ to achieve ~21% efficient cells. This topic will be dealt with in the next chapter.

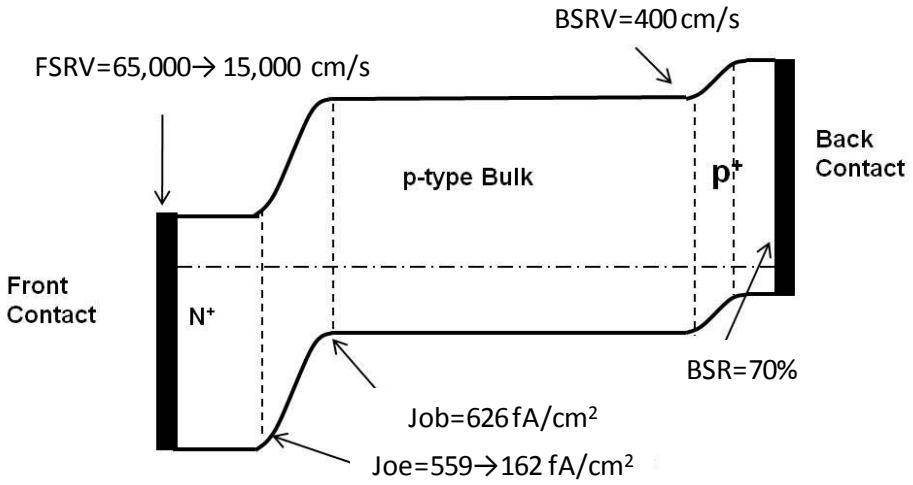



**Figure 5.11 Analysis of $POCl_3$ diffused emitter and ion-implanted selective emitter with Al-local BSF with band diagram**

## 5.5 Summary

This chapter demonstrates the potential and superiority of ion implantation to simplify the production of selective solar cell structure. It also demonstrates several advantages of ion implantation over the conventional $POCl_3$ tube diffusion including single side diffusion, in-situ oxidation for superior surface passivation, elimination of PSG glass removal and junction edge isolation, precise doping control and novel profiles by varying energy, dose and annealing recipes and simplicity of patterned implantation. High efficiency screen printed selective emitter cells with efficiency exceeding 18.8% was demonstrated at the start of this research when state-of-the-art $POCl_3$ emitter cells were 18.3%. The ion-implanted selective cell structure gave 14 mV higher $V_{oc}$, 0.3 mA/cm$^2$ higher $J_{sc}$ and 0.5 % higher efficiency compared to the traditional $POCl_3$ diffused cell. Detailed cell analysis and model calculations revealed that the ion-implanted selective emitter significantly lowered the $J_{oe}$ from 559 fA/cm$^2$ to 162 fA/cm$^2$, while the $J_{ob}$ of the full Al-BSF baseline structure stayed at 626 fA/cm$^2$, which limited the cell $V_{oc}$ and performance. In Chapter 4, our roadmap showed that ~ 21% efficiency cell

will require a much lower $J_{ob}$ of <150 fA/cm$^2$ in conjunction with BSR > 93%. Therefore, a more complex cell structure with passivated and local contacts is developed in this thesis. Next chapter deals with the design and process optimization for the advanced PERC cell to drive the efficiencies close to 21%.

# CHAPTER 6

# DEVELOPMENT OF HIGH EFFICIENCY LARGE-AREA REAR PASSIVATED SILICON SOLAR CELLS WITH LOCAL AL BSF AND SCREEN-PRINTED CONTACTS

## 6.1 Introduction

In the previous chapter, a novel ion-implanted selective emitter cell with full Al-BSF was developed to surpass the efficiency of conventional $POCl_3$ diffused emitter cells. The ion implanted emitter raised the efficiency by 0.5 % absolute, from 18.3 % to 18.8 %, on p-type 239 $cm^2$ Cz Si cells. The in-situ high quality oxide passivation during implantation anneal lowered the FSRV from 65,000 to 15,000 cm/s. Moreover, the lower doping in the emitter decreased the emitter saturation current density to 160 $fA/cm^2$ compared to 560 $fA/cm^2$ for the $POCl_3$ emitter cell. However, PC1D device modeling and analysis (Chapter 4) revealed that the full Al-BSF cell has very high back surface recombination velocity (> 400 cm/s) and low back surface reflectance (~ 70%). Therefore, this chapter presents the understanding and development of a process sequence that incorporates single-side texturing, optimized front and back oxide/nitride surface passivation, appropriate surface finish, and optimally designed local Al back surface field and contacts to overcome the shortcomings of the full area Al-BSF cells. This chapter highlights the importance and optimization of wet chemical etching process for the rear side planarization, which was studied as a function of surface roughness, light trapping and surface passivation quality. The second part of this chapter addresses the optimization of the oxide thickness and its correlation with surface roughness. This was examined by implied $V_{oc}$, oxide charge ($Q_{ox}$) and interface state density or quality (IQF) measurements. This was crucial for eliminating the rear parasitic shunting caused by

inversion layer formation which can short or connect the local contacts. The rear dielectric layer not only needs to provide high quality passivation but should also contain a moderate positive charge density or a high negative charge density to avoid the formation of an inversion layer underneath the oxide. In addition, formation of a high quality and uniform local BSF through the dielectric is also important for preventing the parasitic shunt because BSF tends to become thin around the contact [102]. Finally, a 2-D model is used to optimize the design, size and spacing of rear point contacts to minimize the combined effect of resistive and recombination losses.

## 6.2 Low-Cost Technology Developments to Achieve High Efficiency PERC Cell with Local BSF

Production size 239 $cm^2$ Si cells were fabricated on 160 μm thick p-type boron doped Cz wafers with a base resistivity of 2.5 Ω-cm. Figure 6.1 shows the structure of our PERC or Delta-STAR cell, which has local Al BSF through a passivating rear dielectric. This structure gave cell efficiencies of 20% in our lab on 4 $cm^2$, p-type boron doped FZ silicon wafer with screen-printed contacts [103, 104]. However, several process modifications had to be performed to achieve high efficiency on commercial grade 239 $cm^2$ Cz Si wafers.

First, a process sequence was established to make this structure and then process development and optimization was carried out for each layer to achieve desired properties. The proposed fabrication process begins with saw damage removal in a heated KOH solution followed by alkaline texturing of both sides of the silicon wafers. To investigate the effect of rear surface roughness on the cell performances, one side of the wafers was planarized using different combinations of alkaline solution, etching time and process temperature. In-situ thin oxides were grown on both surfaces during the selective emitter implant anneal which produces 100 Ω/sq emitter in the field and 50 Ω/sq

underneath the grid. To investigate the impact of dielectric thickness on the rear passivation, three different oxide thicknesses in the range of 40-110 Å were grown at 840 ºC and analyzed by a combination of C-V measurements and cell parameters. A PECVD $SiN_x$ film was deposited on the front and rear side to cap the oxide. Then a UV laser (355 nm wavelength with nanosecond pulse width) was used to open vias through the rear dielectric stack. Finally Ag grid was screen-printed on the front and low frit Al on the rear dielectric followed by co-firing in a belt furnace. Notice that the cell had no solderable back pads. Following sections describe technology development associated with each step.

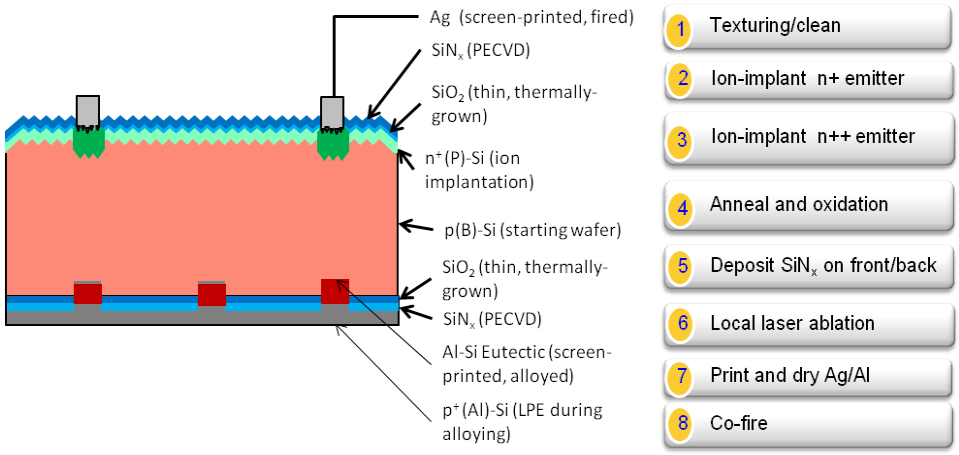



**Figure 6.1 Structure and process sequence of Delta-STAR cell with rear dielectric passivation and point contacts.**

## 6.3 Understanding and Development of Planarized Back Surface Finish for High Quality Rear Side Passivation

The effect of surface roughness of the planarized rear surface was studied using confocal laser microscopy and the long wavelength reflectance measurements. The dielectric passivation was monitored by effective minority carrier lifetime measured by Sinton's QSS-PC method [89]. The oxide charge design ($Q_{ox}$) and interface quality factor (IQF) were extracted from the contactless C-V measurements using a SemiTest SCA-2500 surface charge probe measurements [105].

The Taguchi method was used to design the experiments instead of having to test all possible combinations. The Taguchi method uses orthogonal arrays to organize the parameters that affect the process and the levels at which they should be varied. This allows identification of parameters that have most affect on process quality with a minimum amount of experimentation, thus saving time and costs. The detail information regarding the Taguchi method could be found in the textbook [106].

### 6.3.1 Development and Control of Low-Cost Chemical Etching to Achieve Desired Surface Roughness

According to the model calculations, a BSRV of ~100 cm/s and BSR of ≥ 95% are required to get up to 21% efficiency. This requires some degree of planarization of the back surface. Silicon can be planarized perfectly by polishing but that is a very expensive. Therefore, we decided to develop a simple chemical etching process to planarize the back. A detailed study was conducted to establish what degree of planarization is required and how to achieve it by simple manufacturable chemical treatment.

The experiments were carried out according to the design matrix shown in Table 6.1. The parameters of the alkaline texturing process consist of process temperature,

etching time, and alkaline concentration. The process temperature was varied between 65°C and 80°C; the etching time ranged between 4 minutes to 15 minutes; and alkaline (KOH) concentration was varied between 9% to 17%. The 1's in the parentheses in Table 6.1 represent the low level of each process parameter, whereas 2's represent the high level of each process parameter.

**Table 6.1 L4 table of surface roughness experiment**

| Recipe | Concentration (%) | Time (min) | Temperature (°C) |
|---|---|---|---|
| A | 9 (1) | 4 (1) | 65 (1) |
| B | 9 (1) | 15 (2) | 80 (2) |
| C | 17 (2) | 4 (1) | 80 (2) |
| D | 17 (2) | 15 (2) | 65 (1) |

Figure 6.2 shows the SEM images and confocal laser microscopy of various alkaline etched surfaces in this study. Four alkaline etching recipes resulted in average surface roughness 0.746 μm, 0.496 μm, 0.317 μm, and 0.205 μm, respectively. Textured back surface with no planarization treatment gave 1.3 μm surface roughness. The roughness of the etched surfaces was calculated according to an arithmetic average of the deviation from the mean height roughness according to the following equation

$$R_a = \frac{1}{n}\sum_{i=1}^{n}|y_i| \qquad (6.1)$$

where $R_a$ is the arithmetic average of the absolute values of height $y_i$ and n is the sampling points over an evaluation area of 258 μm × 258 μm.

As can be seen in the confocal profiles and SEM images in Figure 6.2, the choice of planarization process and conditions can significantly affect the roughness of the final surface. A nearly flat surface was obtained using Recipe D which gave average roughness

of only 0.205 μm. These mean values of surface roughness and the relevant process parameters were then used to conduct the main effect analysis by the Taguchi method in order to obtain the optimal process conditions.

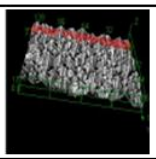
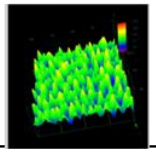
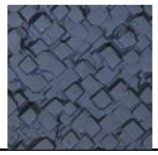
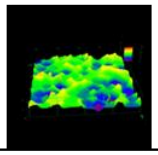
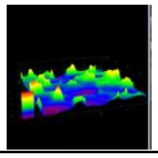
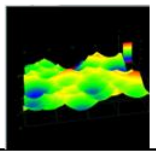
| Recipe | SEM Image | 3D Confocal Profile | Average Roughness (μm) |
|---|---|---|---|
| Double-side Textured |  |  | 1.301 |
| A |  |  | 0.746 |
| B |  |  | 0.496 |
| C |  |  | 0.317 |
| D |  |  | 0.206 |

**Figure 6.2 SEM images and confocal laser microscopy profiles of different alkaline etched surfaces. Average roughness is in unit of micrometer.**

Taguchi analysis of the roughness data in this work was carried out using MINITAB [107], a commercial statistical software. Figure 6.3 shows the main effects plot for each process parameter. The horizontal axis of the plot represents low (1) and high (2) levels of each process parameter while the vertical axis represents the average surface roughness. The data shows that the etching time is the most effective process

parameter to achieve the smallest value of the surface roughness, whereas the process temperature and alkaline concentration are the second and the third ranked process parameter to planarize the wafer surface. According to the Taguchi analysis, the optimal process parameters for a nearly smooth include long etching time (15 minutes), high process temperature (80 ºC) and high alkaline concentration (17%). Next step was to determine the impact of surface reoguness on oxide passivation quality and establish that at best planarization process can attain the desired BSRV value (~100 cm/s).

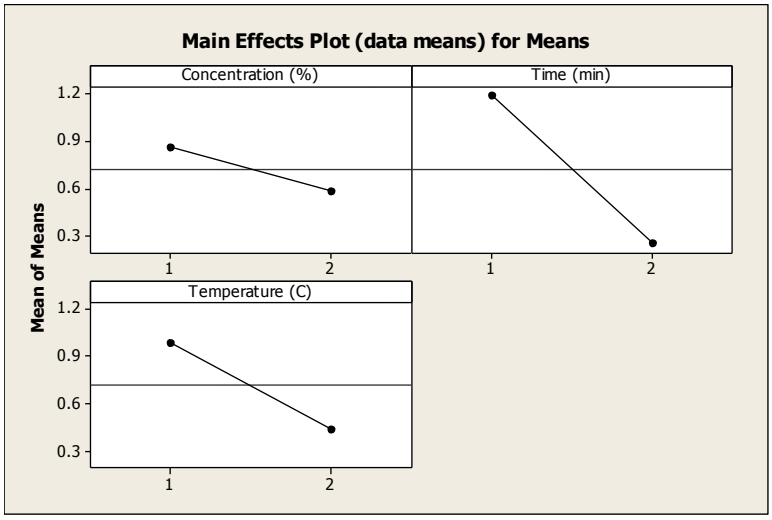



**Figure 6.3 Mean effect plot of the Taguchi analysis.**

### 6.3.2 Impact of the Rear Surface Roughess on Surface Passivation Quality

It is well known that surface finish can have a huge impact on the oxide quality, $Q_{ox}$ and $D_{it}$. Therefore, a study was conducted to evaluate the oxide passivation quality of the chemically etched surfaces. The effective lifetime of symmetrical Cz samples (oxide-Si-oxide) was measured to study the impact of surface roughness on the surface passivation quality. Study was conducted on 180 µm thick 2.5 Ω-cm p-type Cz wafers. Five sets of samples were prepared. On one set of wafers, were etched back for 15 min in

a heated KOH solution using Recipe D, which is the smoothest surface (0.205 µm). Second set of wafers was etched for 25 min to reduce the surface roughness further. In addition, two commercial, inline, wet chemical etching processes from commercial venders were included for comparison. The fifth set involved as-textured wafers with no planarization treatment for reference.

Figure 6.4 shows the resulting surface morphology and surface roughness of the five sets of samples measured by conforcal microscopy. As textured, longer KOH etching time (≥15 min) convert the as-textured wafer surface to nearly polished; however, increasing the etching time (25 min) did not alter the surface finish appreciably beyond 15 min. These oxidized samples were subjected to $SiN_x$ coating deposition and screen print firing simulation to be consistent with the cell processing sequence.

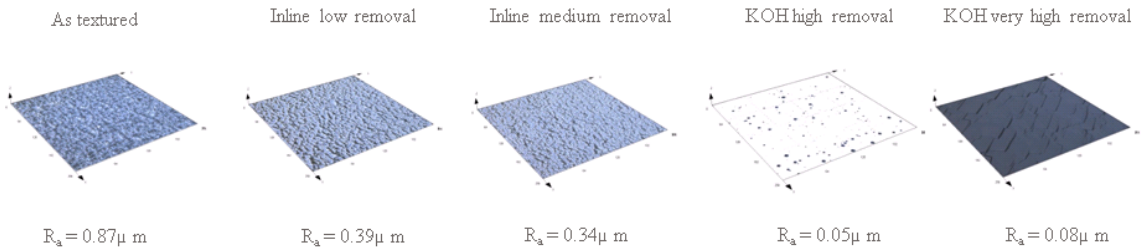



**Figure 6.4 Surface roughness measured by confocal microscopy after different etching processes.**

The effective lifetimes were measured on all five sets after planarization, thermal oxide growth, silicon nitride capping and simulated contact firing at ~750˚C on symmetrically passivated Cz Si wafers. The corresponding surface recombination velocities were calculated from the effective lifetimes [21] and are plotted in Figure 6.5.

Following well known equation was used for surface recombination velocity ($S_{eff}$) calculation [93].

$$S_{eff} = \frac{W}{2}\left(\frac{1}{\tau_{eff}} - \frac{1}{\tau_{Bulk}}\right) \quad (6.2)$$

where

$\tau_{eff}$ : measured effective lifetime

$\tau_{bulk}$: bulk lifetime

$S_{eff}$: effective surface recombination velocity

$W$: wafer thickness

The results show that the effective surface recombination velocity ($S_{eff}$) of as-grown oxide passivated samples decreases with the decrease in surface roughness. After the PECVD-$SiN_x$ coating, the $S_{eff}$ decreased sharply for all the samples. Finally, $S_{eff}$ changed only slightly after the high-temperature contact firing process ~750 ºC, which demonstrates the good thermal stability of the oxide/$SiN_x$ surface passivation stack developed in this work. It is worth noting that after the PECVD $SiN_x$ coating and firing process, there is no consistent relationship between the effective lifetime and the surface roughness. This could be explained by effective hydrogenation of the interface states or by the presence of an inversion layer induced by the high positive charge density in PECVD $SiN_x$. Both effects can help surface passivation but the latter can be detrimental for cells because it can lead to parasitic shunting. In order to gain better insight, complete solar cells were fabricated and evaluated in the following section.

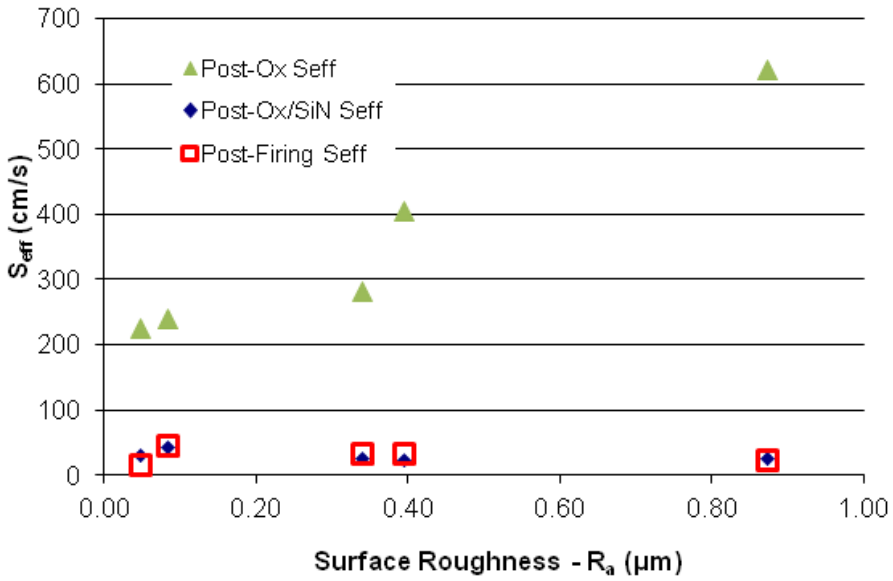



**Figure 6.5 Calculated surface recombination velocities of symmetrically passivated Cz Si samples with different surface roughness.**

### 6.3.3 Impact of the Rear Surface Roughness on PERC Cells

To study the impact of surface roughness on cell efficiency, PERC or Delta STAR solar cells were fabricated using four planarizing etching recipes (A to D), in addition to the textured back surface with no planarization. Oxide thickness was ~90Å. The cell I-V characteristics are listed in Table 6.2. All other process parameters were kept the same. The highest cell efficiency (19.2%) was achieved on the smoothest surface with Recipe D and the textured back surface gave the lowest efficiency (17%). Table 6.2 also shows the cell data for the baseline cell with full Al-BSF with no dielectric passivation. Recipe D gave an open circuit voltage ($V_{oc}$) gain of above 17 mV compared to the baseline full Al-BSF cell and the difference in $V_{oc}$ was only 5 mV for cells with surface roughness of 0.205 and 0.746 µm. It is important to note that the textured back surface performance below the baseline cell with a significant reduction in FF.

Notice that the highest short circuit current was obtained for Recipe A. This is because smaller amount of silicon surface is etched by Recipe A, resulting in slightly thicker (175 μm) cell which absorbs more photons relative to Recipe D which gave 150 μm thick cell. Finally, the increase in the fill factor with decreasing surface roughness had the biggest impact on efficiency. This is attributed to parasitic shunt effect which lowers the FF due to the leakage from the back surface [13]

**Table 6.2 IV results of Cz-Si Delta-STAR cells with differently etched rear surfaces and ~90 Å oxide. The cell area is 239 $cm^2$.**

| Recipe | Surface Roughness [μm] | $V_{oc}$ [mV] | $J_{sc}$ [$mA/cm^2$] | FF [%] | η [%] |
|---|---|---|---|---|---|
| A | 0.746 | 650 | 38.4 | 75.7 | 18.9 |
| B | 0.496 | 652 | 38.1 | 76.4 | 19.0 |
| C | 0.317 | 651 | 38.1 | 76.3 | 18.9 |
| D | 0.205 | 655 | 38.1 | 76.8 | 19.2 |
| Double side Texture | 1.301 | 646 | 37.1 | 74.8 | 17.9 |
| Al-BSF | NA | 638 | 37.0 | 78.8 | 18.6 |

### 6.3.4 Impact of the Rear Surface Roughness on Light Trapping

Besides a BSRV of 100 cm/s, a BSR value of ~95% is required for 21% cells (Figure 4.5). Therefore, in this section, we evaluated the impact of surface finish on BSR. In order to assess the impact of rear surface roughness on light trapping and back surface reflectance, escape reflectance measurements were performed in the long wavelength range ( > 1000 nm). Higher escape reflectance is indicative of superior BSR, which could give added boost in $J_{sc}$. Figure 6.6 shows the long wavelength reflectance for the different

surface roughnesses. The escape reflectance of full Al-BSF cell is also shown in the figure for comparison. It can be seen that the smoothest surface (Recipe D) has the highest escape reflectance while for full Al-BSF cell has the smallest escape reflectance. The planarization study highlights the importance of having an optimized rear surface as it affects all I-V parameters and the optical performance of the solar cell. PC1D device modeling program was used to extract the BSR value by matching the calculated and measured escape reflectance. The analysis gave a BSR value of ~70% for the conventional full Al-BSF cell and ~93% for the Recipe D cell. Notice that cell D has 0.3 $mA/cm^2$ lower current compared to cell A, in spite of superior BSR. This is because cell D is 20 µm thinner than cell A, which results in ~0.5 $mA/cm^2$ less in Jsc, otherwise cell D would have been even higher than 19.2%. In conclusion, planarization recipe D developed in this research is capable of giving BSRV of ~100 cm/s and BSR of ~93%.

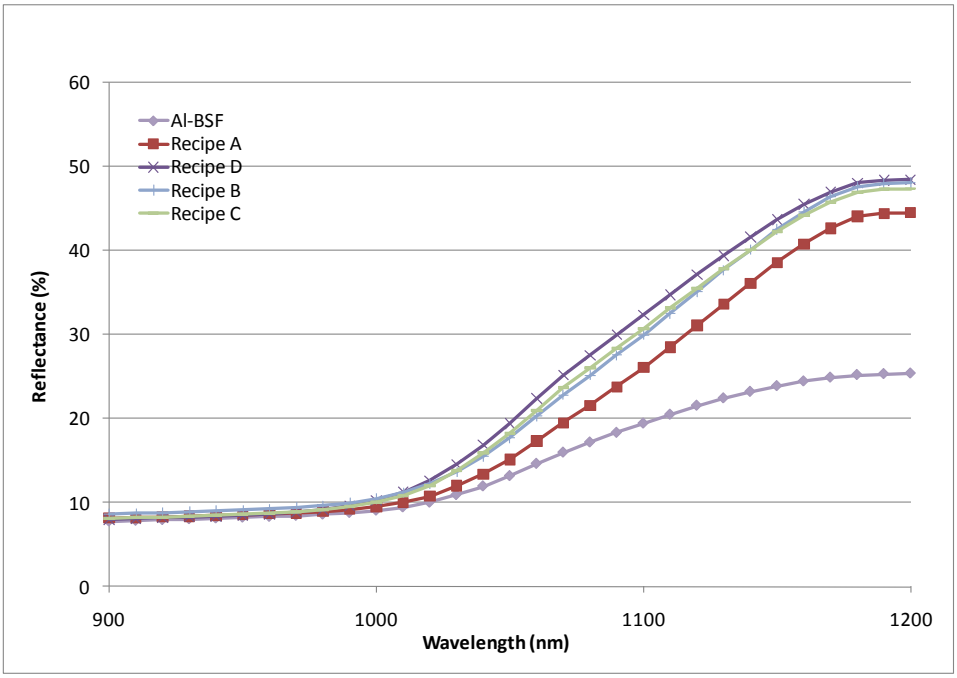



**Figure 6.6 Impact of surface finish on long wavelength escaped reflectance.**

## 6.4 Development of a Low-Cost Dielectric Stack for Effective Rear Surface Passivation and Reflector of PERC Cell

Thermally grown silicon dioxide has been extensively investigated for the surface passivation of solar cells. Surface passivation is generally a function of surface and oxide thickness. Therefore, in an effort to improve surface passivation in this section, we have studied the combined effect of the rear surface roughness and oxide thickness on surface passivation. This is done by using surface morphologies developed in the previous section in combination with three different oxide thicknesses in the range of 40-110 Å. The fixed oxide charge and interface quality factor (which is proportional to the density of interface state) were measured since they are the key to the performance of dielectric passivated local Al-BSF solar cells. A low density of interface state gives superior passivation. A modest positive charge density ($< 2\times10^{11}$ $cm^{-2}$) also improves the passivation quality but brings an increased risk of parasitic shunting if charge density becomes too high to form an inversion layer at the silicon/dielectric interface. Therefore, optimizing the back dielectric that can provide good passivation without shunting the finished cell was an important task in this thesis. The dielectric passivation was monitored by using the Sinton's QSS-PC tool on a symmetric test structure on a p-type ~2 Ω-cm Cz Si wafer. The combined effect of the oxide thickness and surface roughness on passivation quality is also investigated on advanced cells.

### 6.4.1 Measurement and Analysis of Fixed Oxide Charge and Interface Quality Factor in Thermally Grown Back Oxides

To examine the effect of oxide thickness on passivation, three different oxide thicknesses were grown on wafers with mirror-polished surface. The oxidations were carried out in dry oxygen ambient with 3% dichloroethene (DCE) at 840ºC. Oxidation

times were 5 minutes, 30 minutes and 55 minutes which resulted in 40 Å, 90 Å and 110 Å thick thermal oxides. The oxide thicknesses were measured with an ellipsometer.

To understand the passivation properties of these oxides, the density of the fixed oxide charge ($Q_{ox}$) and interface states ($D_{it}$) were extracted by contactless C-V measurements using a SemiTest surface charge analyzer (SCA-2500). The interface state density for our samples was outside the measurement range of the SCA-2500, which in such situations, provides an interface quality factor (IQF) instead of $D_{it}$ to characterize the interface. IQF is given by

$$IQF = \frac{dQ_{ind}}{dQ_{sc}} = \frac{1}{qN_{sc}} \frac{dQ_{ind}}{dW_d} \tag{6.3}$$

which is related to the interface state density by

$$D_{it} = \frac{\varepsilon_s}{q^2 W_d} (IQF - 1) \tag{6.4}$$

The parameters used in Equation (6.3) and (6.4) are defined as follows:

$Q_{ind}$ : induced charge

$Q_{sc}$ : semiconductor space charge

$q$ : elementary charge of an electron

$N_{sc}$ : doping concentration

$W_d$ : surface delpetion width

$\varepsilon_s$ : permitivity of dielectric

The IQF lies between 0 and 100. A value of 0 represents a perfect interface while a value of 100 represents the worst interface between silicon and silicon oxide. A detail of description of the theory behind the SCA-2500 measurements can be found in [105]. Figure 6.7 shows the $Q_{ox}$ and IQF for the three oxides grown in this study. The thicker

oxide gave a higher fixed oxide charge density and lower interface factor, both are good for passivation. Modestly high fixed oxide charge results in good field-effect passivation; however, too much positive charge (> $2\times10^{11}$ /$cm^2$ ) may cause inversion at the dielectric/silicon interface and lead to a parasitic shunt [13].

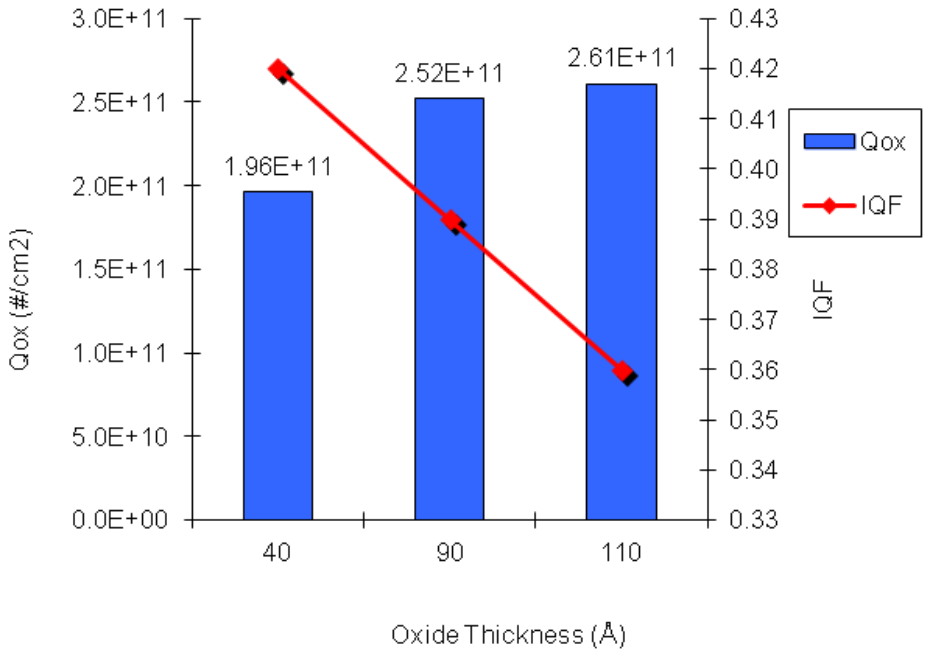



**Figure 6.7 Dielectric charge, and interface quality factor as a function of rear oxide thickness.**

### 6.4.2 Surface Passivation Quality of Thermally Grown Rear Oxides

In order to quantify the quality and thermal stability of the oxide layers, symmetric test structures were fabricated to measure effective lifetime (Figure 6.8). Double-side textured wafers were planarized by etching for 15 min at 80˚C (Recipe D in previous section) followed by thermal oxidation to passivate both sides of the wafer. The oxide layers were then capped with a 500 Å thick PECVD $SiN_x$ layer and subjected to a high

temperature contact firing cycle to simulate the cell fabrication sequence without metallization.

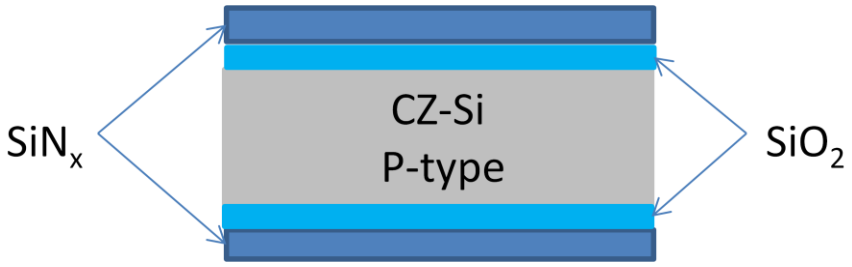



**Figure 6.8 Schematic of test structure used for lifetime measurements.**

Figure 6.9 shows the change in surface recombination velocity for the 90 Å oxide after each process step. The surface recombination velocity S was calculated using the Equation (6.5):

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{2S_{eff}}{W} \qquad (6.5)$$

where $\tau_{eff}$ and $\tau_{bulk}$ are the effective and bulk lifetime, measured by QSS-PC and $W$ is the wafer thickness. The $S_{eff}$ value for the as-grown 90 Å oxide was 187 cm/s which reduced to 122 cm/s after the $SiN_x$ deposition and increased slightly to 136 cm/s after the firing process. Note that this is more than a factor of three smaller than the BSRV value of 400 cm/s for the full Al-BSF baseline cell. This should lead an to appreciable increase in $V_{oc}$ of the dielectric passivated rear contact cell compared to the baseline cell.

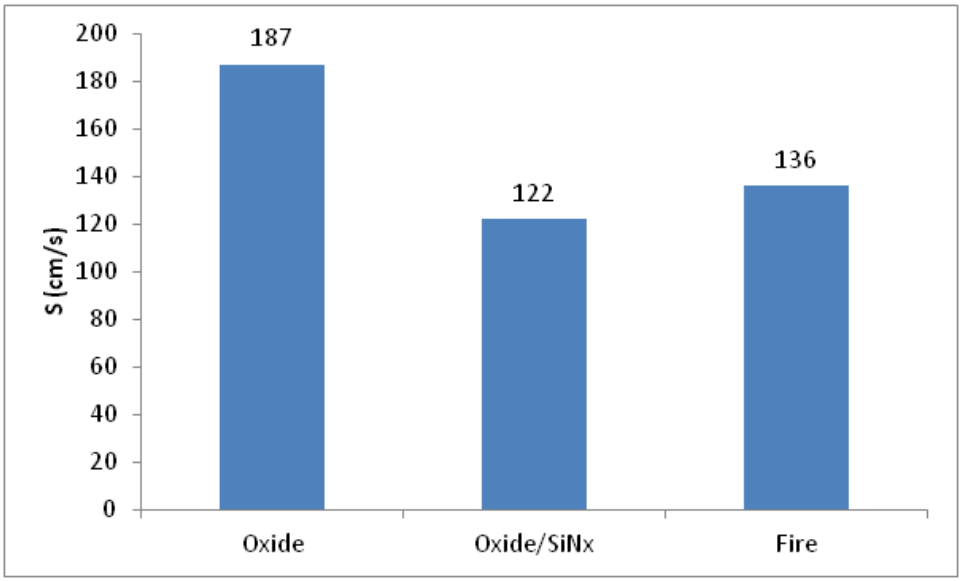



**Figure 6.9 Change in surface recombination velocity of un-metalized dielectric passivated sample.**

### 6.4.3 Fabrication of Screen-Printed Dielectric Back Passivated Solar Cells

After establishing the thermal stability of the oxide/nitride stack, a study was conducted to find the best combination of surface roughness and oxide thickness for cell performance. Two different surface finishes were prepared using recipes A and recipe D (Table 6.1) and the above three oxides were grown on the back surface and capped with $SiN_x$ film. Complete Delta STAR cells were fabricated and analyzed using the process sequence described earlier in Section 6.2. Table 6.3 shows that 19.4% efficient Delta-STAR cells (239 $cm^2$) were achieved on 2.2 Ω-cm Cz Si with smoother rear surface and 90Å $SiO_2$/PECVD $SiN_x$ stack. Both the surface morphology and the oxide thickness were found to be important. In general, thicker dielectric and smoother surface provide better passivation. In addition, a thicker oxide reduces the sensitivity to surface roughness. Note that 90 Å oxide gave the best cell performance because thicker back oxide results in much thicker front oxide (oxide grows much faster on $n^+$ Si than p-Si) which affects the anti-reflection coating on the front and lowers the short circuit current. Therefore,

PECVD $SiN_x$ on the front needs to be optimized to gain the full benefit of high quality rear-surface passivation with a thicker oxide. Detailed optical modeling is performed later on (Chapter 8) to tailor the $SiN_x$ thickness to achieve best back passivation as well as low front surface reflectance.

**Table 6.3 IV results of Cz-Si Delta-STAR cells with differently etched rear surfaces and different dielectric thickness. The cell area is 239 $cm^2$.**

| Oxide [Å] | Surface | $V_{oc}$ [mV] | $J_{sc}$ [$mA/cm^2$] | FF [%] | η [%] |
|---|---|---|---|---|---|
| 40 | rough | 640 | 37.6 | 74.6 | 18.0 |
| | smooth | 641 | 37.7 | 76.0 | 18.4 |
| 90 | rough | 652 | 38.4 | 77.0 | 19.3 |
| | smooth | 656 | 38.1 | 77.8 | 19.4 |
| 110 | rough | 644 | 38.1 | 77.3 | 19.0 |
| | smooth | 643 | 37.9 | 76.7 | 18.7 |

### 6.4.4 Quantitative Understanding and Analysis of Screen-Printed Dielectric Back Passivated Solar Cells

In order to explain the difference between baseline and PERC cells quantitatively, reflectance and IQE measurements were performed on an 18.6% efficient full Al-BSF cell and a 19.3% efficient local BSF cell passivated with a 90 Å thick rear oxide. It is clear that dielectric back passivated Delta-STAR cell has much higher BSR and lower BSRV, as indicated by higher escape reflectance ($\lambda > 1000$ nm) and long wavelength IQE ($\lambda > 900$ nm) response in Figure 6.10. PC1D modeling was used to match of the experimental I-V and IQE data to extract BSRV and BSR values. This analysis revealed a significant increase in BSR value from 71 to 93% and a substantial decrease in BSRV

from 400 to 130 cm/s. It is important to note that an excellent match was achieved between the experimental data and modeling when a rear surface charge density of $2\times10^{11}$ $cm^{-2}$ was used, which is consistent with the measured oxide charge density.

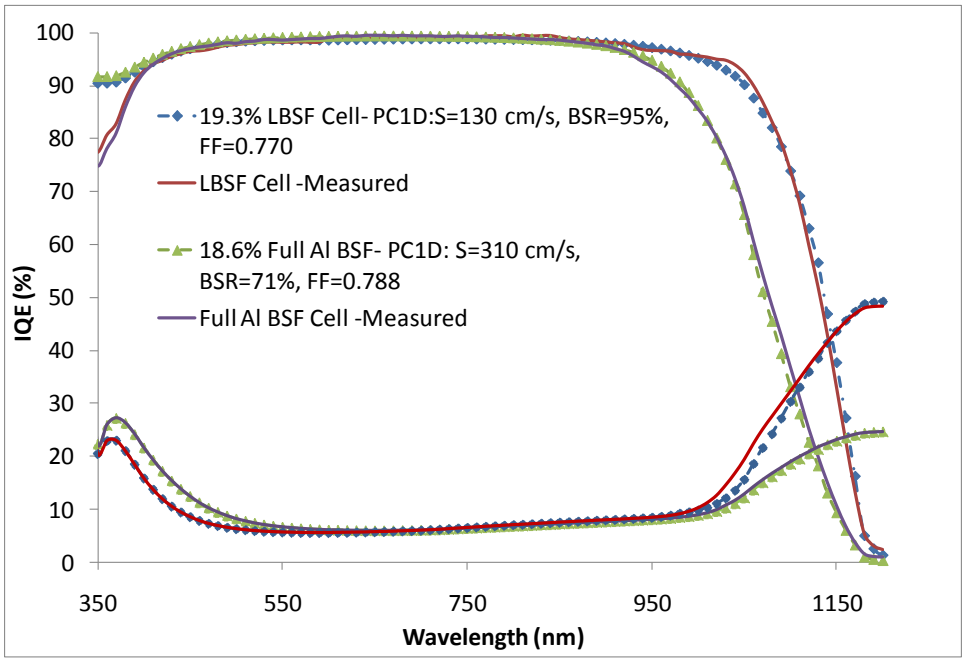



**Figure 6.10 IQE and reflectance comparison of Delta-STAR and Al-BSF cell. (Solid lines represent measured IQE and reflectance.)**

## 6.5 Design optimization and Fabrication of Local Contact through Back Dielectric Stack for Achieve High Efficiency

The above cells were fabricated with 130 µm × 130 µm vias with a pitch of 800 µm which was found to be the source of low FF (77.0%) in the 19.3% cell. Therefore, we followed the guidelines established by Meemongkolkiat [13] using a 2-D device model to establish the right combination of the rear contact spacing and opening for the vias. The solar cell efficiency, $J_{sc}$, $V_{oc}$ and FF values were calculated by Meemongkolkiat [13] as a function of contact spacing and SRV values for 75 µm and 150 µm wide square shaped contacts. Simulations showed that the optimal spacing is smaller for a smaller contact width and the optimal spacing increases with the increase in the effective SRV at the p-p+ interface recombination. This is because optimal spacing is the result of the competition between the resistive and the contact recombination losses [13]. Increasing the spacing increases the resistive loss but decreases the contact recombination, which in turn increases the series resistance and $V_{oc}$ but lowers the fill factor. His calculations gave an optimal spacing of 500 µm for the 150 µm × 150 µm square openings for a good passivation. Figure 6.11 shows the corresponding experimental data generated in this research for ~130µm × 130 µm vias as a function of spacing. Consistent with the model, the best cell performance of 19.6% was achieved at 500 µm spacing for our cells with a BSRV of 130 cm/s and $Q_{ox}$ of $2\times10^{11}$ $cm^{-2}$. Table 6.4 shows the cell data of several 19.3% to 19.6% efficient Delta STAR cells fabricated with the optimized parameters, namely 0.205 µm surface roughness, 90 Å oxide thickness, and 500 µm spacing for 130 µm wide square contacts.

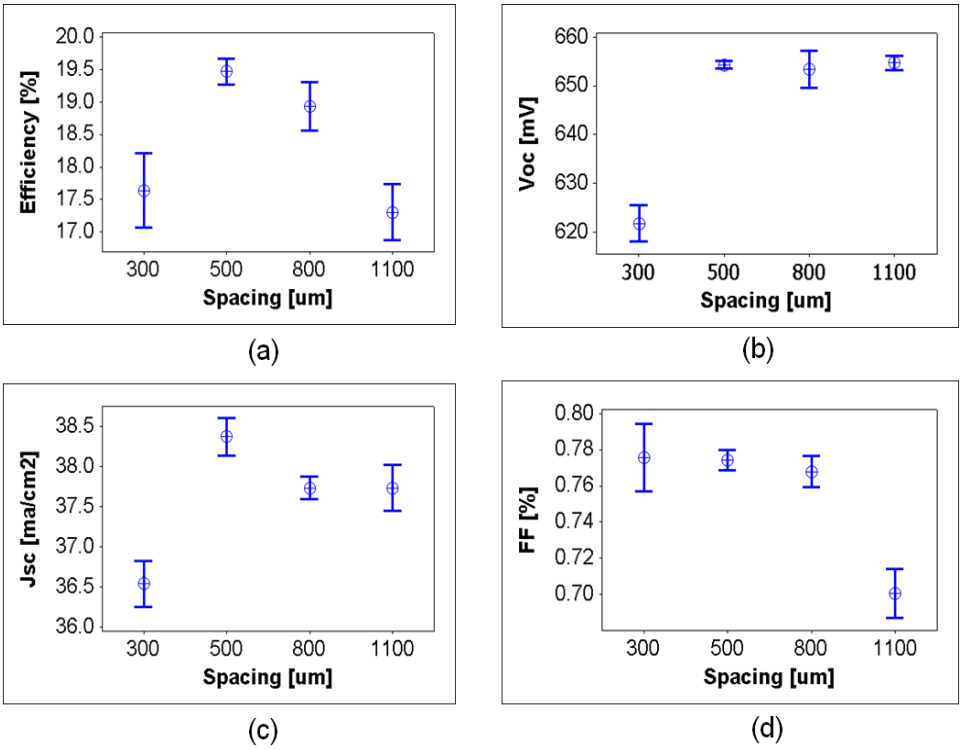



**Figure 6.11 Experimental data for 239 cm$^2$ Delta-STAR cells with 130 μm contact width and various contact spacing. Each contact spacing contains five cells.**

**Table 6.4 List of 19.3%-19.6% of Delta STAR Cells**

| ID | $V_{oc}$ [mV] | $J_{sc}$ [mA/cm$^2$] | FF [%] | η [%] |
|---|---|---|---|---|
| S-1 | 656 | 38.5 | 77.8 | 19.6 |
| S-2 | 654 | 38.3 | 77.7 | 19.5 |
| S-3 | 654 | 38.2 | 77.0 | 19.3 |
| S-4 | 654 | 38.5 | 77.2 | 19.5 |
| S-5 | 655 | 38.3 | 77.6 | 19.5 |
| S-6 | 655 | 38.2 | 77.2 | 19.3 |
| S-7 | 655 | 38.6 | 77.4 | 19.6 |
| Average | 655 | 38.4 | 77.4 | 19.5 |

## 6.6 Summary

This chapter shows quantitatively that back surface finish, rear oxide thickness, dielectric charge and interface quality, and local BSF design, all play an important role in providing excellent back passivation without parasitic shunting. This know-how was applied to fabricate cells with all the optimized parameters, namely 0.205 µm surface roughness, 90 Å oxide thickness, and 500 µm spacing for 130 µm wide square contacts. This resulted in 19.6% efficient, 239 $cm^2$ screen-printed Cz Si solar cells with the $V_{oc}$ of 656 mV, $J_{sc}$ of 38.5 $mA/cm^2$ and FF of 77.8%. This rear dielectric passivation and contact scheme improved the BSR value form 70% to 93% and lowered the BSRV from 400 to 130 cm/s relative to the full Al-BSF reference cell. This was one of the highest efficiency screen-printed 239 $cm^2$ p-type LBSF Cz Si solar cells in 2011.

Model calculations in Chapter 4 showed that the gridline shading must be less than ~6% for achieving ~21% efficiency target. Therefore, the next chapter will focus on the implementation of a novel fine-line direct printing technology that provides narrow grid lines with high aspect ratio.

# CHAPTER 7

# IMPLEMENTATION OF A NOVEL FINE-LINE DIRECT PRINTING TECHNOLOGY TO ACHIEVE HIGH EFFICIENCY PERC CELLS

Screen-printed silicon solar cells currently dominate the commercial market because of their simplicity and lower manufacturing cost. However, commercial screen-printing technology poses some limitations for higher efficiency cells. The primary disadvantages are wider lines (which increases shading loss and reduces the short-circuit current) and lower aspect ratio (which increases grid line resistance and lowers FF). In addition, screen-printing introduces stress during printing due to physical contact with squeeze and screen which can break thin wafers.

Therefore, this chapter investigates a novel, non-contact, direct printing technology that results in narrow lines and high aspect ratio. This technology was developed by nScrypt Corporation and is similar to extrusion printing where the paste is applied through a nozzle to write the grid pattern without the use of screen. The performance of advanced cells with direct printing and screen printing are compared. Detailed modeling and analysis is performed to determine the components of series resistance in the screen-printed and direct printed cells. Finally, grid modeling is extended to optimize the grid design this non-contact printing technology to get the maximum benefit of fine lines.

## 7.1 Introduction to Direct Printing Technology

In the study, a novel nScrypt direct printing technology was used for printing the front grid lines of the PERC solar cell. This technologies is now well documented in the literature [108, 109] and is similar to extrusion printing with no direct contact between the dispersive tip and the wafer. This section highlights few key features of the direct printing technology relevant to this thesis. The nScrypt direct printing technology is based on the micro-dispensing method that passes the screen printable paste through a micro nozzle for printing the gridline. Figure 7.1 shows the schematic drawing of nScrypt SmartPump$^{TM}$ valve which has the ability to dispense material with wide range of viscosities from 1 centipoise (cps) to several million cps. Thinner liquids, such as water, have lower viscosities, while thicker liquids like oil have higher viscosities. Typically the conductive silver paste used in the direct printing technology is modified to have a high viscosity in order to improve the resolution and accuracy of printing. The nozzle has been optimized to a conical shape which reduces the pressure needed to extrude the highly viscous conductive pastes, thus the flow rate can be increased at the same pressure level as compared to standard tubing tip. The paste is transferred from a cartridge by applying positive pressure through the material-flow inlet into the valve. When dispensing starts, the valve opens and then the paste flow through the nozzle onto the Si substrate. The open and close of the valve is controlled by the position of the valve rod in the center of the SmartPump$^{TM}$ assembly. The flow rate of the paste is governed by the rhoelogy of the paste, the feed-in pressure, the valve opening, the nozzle size and the dispensing gap between the nozzle and the substrate.

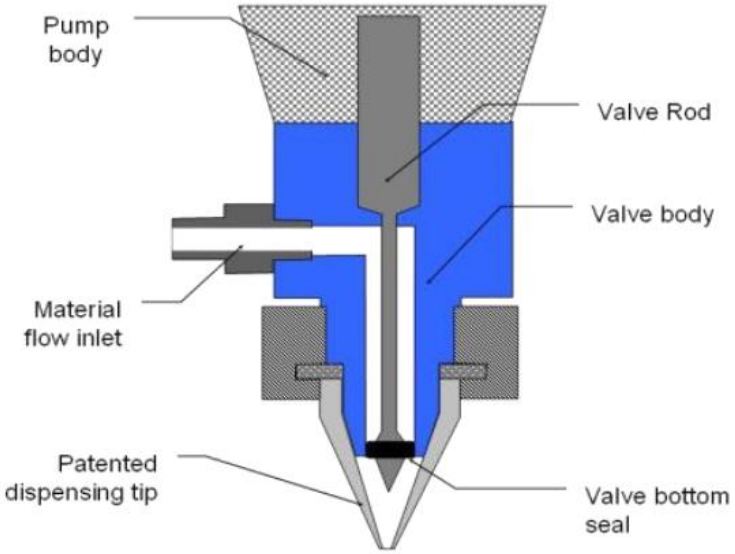



**Figure 7.1 Schematic drawing of nScrypt SmartPump$^{TM}$ valve assembly [108].**

An nScrypt 3Dn-450 Direct-Printing lab-type tool integrated with the SmartPumpTM, and a high precision and high speed motion platform was used for the front side metallization process. The working stage can fit production size silicon solar cells. The grid pattern designed in the CAD software was imported into the computer system in a DXF formant. The system compiles several types of commands to control the printing process. A set of printing parameters, such as printing gap, air pressure, valve opening, and motion speed can be programmed into the computer system.

Figure 7.2 shows the schematic illustration of the direct printing (non-contact) process. The modified silver paste is fed into the pump. By controlling the positive pressure, the nozzle dispenses the paste directly on the silicon substrate. The positive pressure is created by compressed air with high resolution of 0.1 psi. The gap between the nozzle and the wafer surface is more than 75 μm which is tolerable for any cell thickness and any surface roughness. Note that the nozzle does not contact with the wafer surface, therefore, the high aspect ratio grid line can be formed by this novel printing

technology. To meet the requirement of mass production in the solar industry, multi-nozzle head and its array is being developed in nScrypt Inc.

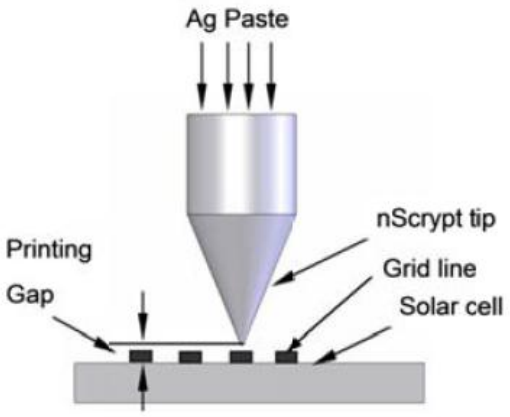



**Figure 7.2 Schematic drawing of direct printing for gridline printing [108].**

## 7.2 Experimental Demonstration of Efficiency Enhancement from Direct Printing Technologies

Commercial size 239 $cm^2$ Si cells were fabricated on 160 μm thick p-type boron doped Cz wafers with a base resistivity of 2.5 Ω-cm. Figure 7.3 shows the structure of the PERC cell with local Al-BSF, which gave cell efficiencies of ~19.6% with conventional screen-printed contacts in Chapter 6. At that time (2012) in this research, the width of the front screen-printed lines was about 100μm, resulting in ~8% shading. Our technology roadmap in Chapter 4 showed that gridline shading needs to be ≤ ~6% for achieving ~21% efficient cells.

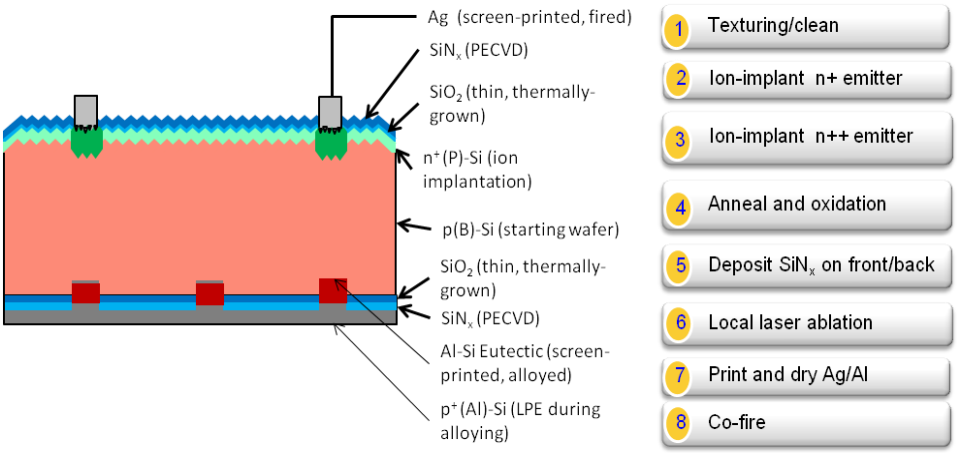



**Figure 7.3 Structure and process sequence of Delta-STAR cell with rear dielectric passivation and point contacts.**

### 7.2.1 Fabrication and Comparison of PERC Cells with Screen-Printing and Direct-Printing Technologies

The fabrication process begins with saw damage removal in a heated potassium hydroxide solution (chemical formula:KOH) followed by alkaline texturing of both sides of the silicon wafers. Front side of the wafers was protected by a dielectric while the back side was planarized using alkaline solution. In this study selective emitter was formed by ion implantations. First, the entire wafer was implanted with a lower dose to create the high sheet resistance field region. A proximity mask was then inserted between the wafer and the ion beam without removing the wafer, and a second implant followed. Openings in the mask define a grid-pattern of heavily doped regions to which the front screen printed contacts are aligned. The implant damage was annealed in a tube furnace. Implantation energy, dose and anneal conditions were selected to achieve 100 Ω/sq sheet resistance in the field and ~50 Ω/sq under the grid area of the selective emitter. In-situ thin oxides was grown on the front and rear surfaces during the implant anneal and capped with appropriate SiNx coating prior to forming the screen printed contacts. A

laser was used to open vias through the rear dielectric stack followed by either screen printing or direct printing of Ag grid on the front. A commercial Al paste with lower frit content was screen-printed on the rear of all the wafers. Finally both the contacts were co-fired in a conventional belt furnace to form the grid contact on the front and a local Al-BSF in the rear.

Conventional screen-printing was performed using DuPont PV 17X paste and a semi-automated ASYS printer. The screen-printed Ag grids were formed using a high tension (> 30 N), 290 mesh steel wire screen with 0.8 mil emulsion thickness and 80 µm gridline openings. For the 100 Ω/sq sheet resistance and 239 $cm^2$ cell area, 74 gridlines with three busbars were applied, resulting in an average gridline width of 100 µm and height of 28 µm.

For the direct printing technology, first the three busbars were screen printed. Then, at nScrypt, the gridlines were directly printed over the busbars using a pen tip with only 50µm orifice. Since the expected line width was ~55µm, grid model calculations [17, 110] revealed that 83 lines are optimum for direct printing technology. Therefore, we printed some cells with 74 as well as 83 lines using a version of PV17X modified for direct printing. The gap between the pen tip and the silicon wafer was more than 75µm, and the material feed-in pressure was less than 100 psi. The programmed printing speed was more than 200mm/s. The method for contact co-firing employed fast temperature ramping and short dwell time at the Ag grid sinter point to foster low Ag/Si contact resistance and promote formation of uniform Al back surface field [111].

### 7.2.2 Impact of Novel Direct-Printing Technology on PERC Cell Performance

Generally, fewer lines result in reduced shading loss but that can lead to higher sheet resistance loss because carriers have to travel more distance to be collected by the grid. That is why we fabricated direct printed cells with 74 gridlines as well as 83 gridlines, compared to reference screen printed cells with 74 gridlines. The I-V characteristics for all three cells are listed in Table 7.1. The light I-V data represents an average of the best five solar cells for each condition. The cell efficiency of 20.2% was achieved using direct printing of 83 gridlines compared to 19.7% screen printed cells with 74 lines. The 20.2% direct printed cell had a $V_{oc}$ of 657mV, $J_{sc}$ of 38.4 mA/cm$^2$ and FF of 80.0%, indicating an improvement in $V_{oc}$, $J_{sc}$, FF (Table 7.1). Short-circuit current is improved because of less shadowing loss compared to conventional screen printed cells, and FF and $R_s$ are improved because of optimized grid design. Notice that the open-circuit voltage was higher for direct printing partly because reduced metal coverage results in reduced carrier recombination in the emitter and lower emitter saturation current ($J_{oe}$). Note that the direct printed cell with unoptimized 74 grid lines gave an efficiency of only 19.6% due to higher series resistance and lower FF. This study highlights the importance of fine line printing and optimization of grid design for the fine line printing. In summary, an approximately 0.5% improvement in absolute conversion efficiency was achieved via direct printing of Ag grid on advanced cell structure.

**Table 7.1 Average I-V parameters of solar cells with screen-printed and direct-printed Ag gridlines.**

| Parameter | Screen-Printed (74 gridlines) | Direct-Printed (74 gridlines) | Direct-Printed (83 gridlines) |
|---|---|---|---|
| $V_{oc}$ (mV) | 655 | 655 | 657 |
| $J_{sc}$ (mA/cm$^2$) | 38.1 | 38.6 | 38.4 |
| FF(%) | 78.7 | 77.7 | 80.0 |
| Eff. (%) | 19.7 | 19.6 | 20.2 |
| $R_s$ (Ω-cm$^2$) | 0.76 | 0.87 | 0.44 |
| $R_{sh}$ (Ω-cm$^2$) | 18161 | 6577 | 23876 |
| Line Width (μm) | 100 | 55 | 55 |
| Line Height (μm) | 28 | 38 | 38 |
| Grid Shading (%) | 7.6 | 5.5 | 5.8 |

### 7.2.3 Detailed Characterization and Series Resistance analysis of Direct Printed Contacts

Figure 7.4 shows representative Keyence microscope images of both screen-printed and direct printed PV17X gridlines. The microscope allows three dimensional imaging of gridlines, which visually contrasts the aspect ratios of the different printed method. The height-to-width aspect ratios of the screen-printed and direct printed gridlines are 0.28 and 0.69, respectively. Screen printed lines were 100μm wide and 28 um tall, while the direct printed lines were 55μm wide with a 38μm height.

Using the method of Meier, et al. [112], total series resistance ($R_s$) was broken down into six components: busbar, gridline, Ag/Si contact, sheet resistance, bulk Si, and back contact (Figure 2.10). Each component of $R_s$ is listed in Table 7.2 for the three cells: (a) screen printed cell with 74 lines, (b) direct printed cell with 74 lines, (c) direct printed cell with optimized 83 lines. Note that the sum of components agrees well with the total $R_s$ obtained from the light I-V measurements (Table 7.1). Notice that the direct printed grid pattern with 74 lines gave higher grid line resistance than the screen printed cell. Therefore, in spite of the gain in $J_{sc}$, efficiency did not increase. However, the direct

printed with optimized 83 lines gave much smaller sheet resistance and gridline resistance loss compared to the screen printed patter. This led to an appreciable decrease $R_s$ (0.44 Ω-cm$^2$), much higher FF (0.800), higher $J_{sc}$ (38.4 mA/cm$^2$), and ~0.5% increase in cell efficiency compared to the commercial screen printed cell.

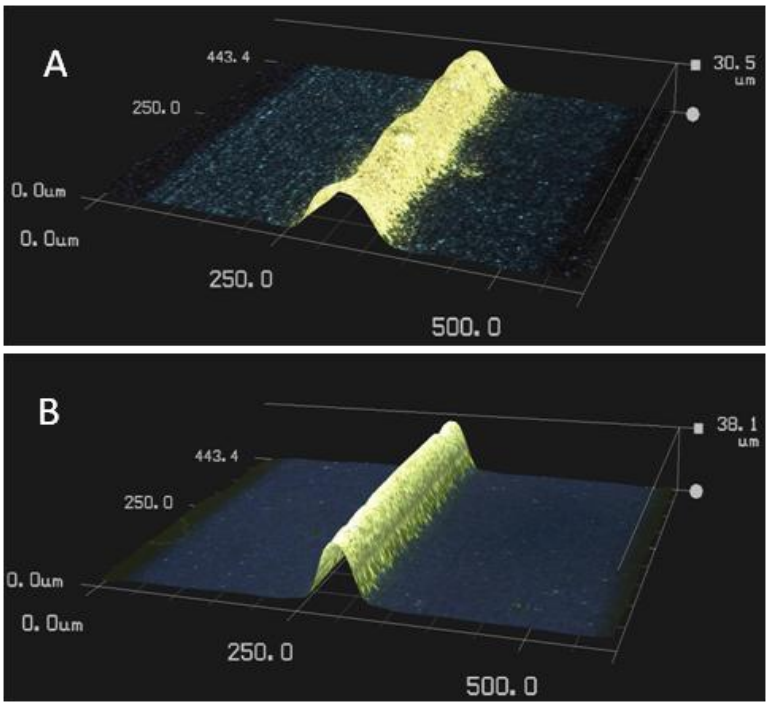



**Figure 7.4 Keyence microscope images of (A) screen-printed Ag gridline and (B) direct printed Ag gridline.**

**Table 7.2 comparison of series resistance components for Delta STAR cells with screen printed and direct printed Ag gridlines.**

| Component (Ω-cm$^2$) | Screen-Printed (74 gridlines) | Direct-Printed (74 gridlines) | Direct-Printed (83 gridlines) |
|---|---|---|---|
| rs(busbar) | 0.0033 | 0.0035 | 0.0035 |
| rs(gridlines) | 0.2626 | 0.2828 | 0.2521 |
| rs(emitter sheet) | 0.3234 | 0.3234 | 0.2579 |
| rs(substrate) | 0.0357 | 0.0357 | 0.0357 |
| rs(back contact) | 0.0795 | 0.1594 | 0.0447 |
| rs(front contact) | 0.0431 | 0.0431 | 0.0431 |
| $R_s$(Total) | 0.7478 | 0.8479 | 0.6370 |

## 7.3 Summary

Implementation of the novel nScrypt direct printing technology and DuPont Solamet® PV17X Ag paste resulted ~0.5% absolute efficiency improvement over the commercial screen-printed cells. This gave the PERC cell efficiency from 19.7% to 20.2%. The improvement in efficiency came from decreased emitter shading and optimized grid design that decreased emitter sheet resistance loss without increases shading. This resulted in higher FF, lower $R_S$ and higher $J_{sc}$. An aspect ratio of 0.69 was achieved with direct printing with a line width 55 µm and height of 38 µm compared to the aspect ratio of 0.28 for the commercial screen-printed contacts with the line width of 100 µm and height of 28 µm. Detailed analysis of $R_s$ demonstrated that direct printed solar cells with optimized grid pattern have appreciably lower emitter sheet resistance and gridline resistance losses compared to their screen-printed counterpart. The direct printed cells with 83 gridlines resulted in 20.2% efficient Cz cells with the $V_{oc}$ of 657 mV, $J_{sc}$ of 38.4 mA/cm$^2$ and FF of 80.0%. This was one of the highest efficiency screen printed 239 cm$^2$ p-type oxide/nitride passivated LBSF Cz Si cell in 2012 [15].

The above cells were fabricated with ion-implanted selective emitter, which requires heavy doping under the gridlines for good ohmic contact and low doping in between the gridlines to reduce emitter recombination. This helps in increasing efficiency, however, the highly doped 500µm wings tend to lower the blue response, and increase surface and Auger recombination. In addition, the selective emitter increases processing cost and reduces throughput due to two different doping levels and the alignment of printed gridlines onto the wings. Moreover, the nScrypt technology was not ready for commercial use at that time. In addition, we also experimented with emerging silver pastes that enable good screen printed contact to higher sheet resistance emitters without significantly increasing the contact resistance. Furthermore, we were able to improve screen-printing technology with the new Ag pastes and new screen design with

narrow openings to shrink the screen printed line width from 100 μm to 80 μm. This technology development resulted in 20.0% screen-printed GEN-I PERC cells with the $V_{oc}$ of 656 mV, $J_{sc}$ of 38.3 mA/cm$^2$ and FF of 79.5%. These parameters will serve as reference for the development of the GEN-II PERC cell in the following chapter.

# CHAPTER 8

# DEVELOPMENT OF HIGH EFFICIENCY ~21% LOW-COST MANUFACTURABLE PERC CELLS WITH HOMOGENEOUS EMITTERS

In the previous chapters, we raised the efficiency of $POCl_3$ diffused baseline 18.3% efficient cell to 20.2% GEN-I PERC cell by a combination of ion implanted selective emitter, optimized back surface finished, dielectric back passivation, optimized size of spacing of local Al-BSF, improved Ag printing and firing, and fine line direct printing technology (Figure 8.1).

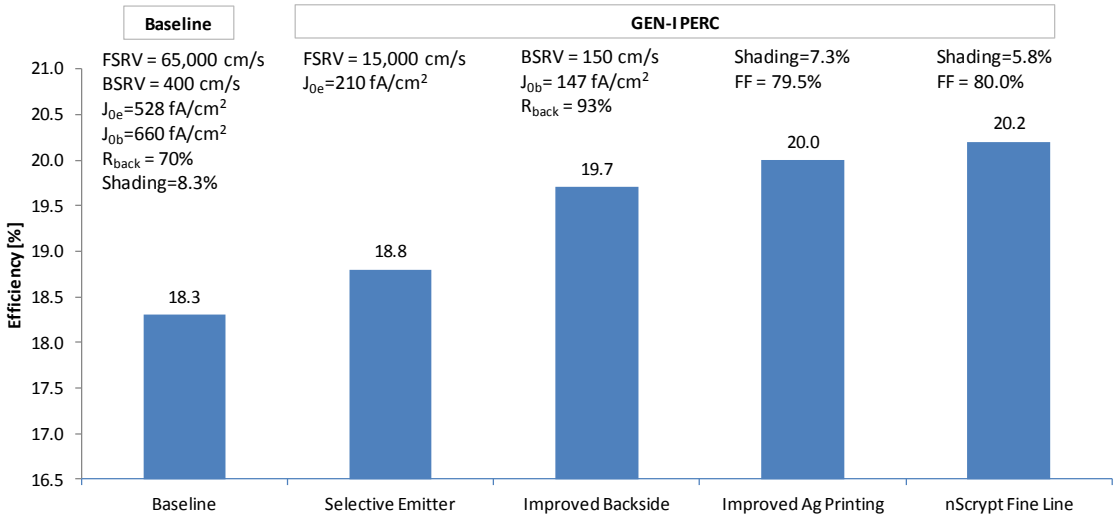



**Figure 8.1 Evolution of the efficiency of GEN-I PERC silicon solar cells.**

In this chapter, we propose to raise the PERC cell efficiency closer to 21% by a combination of fundamental understanding of loss mechanisms, process and design

optimization, technology innovation and complete fabrication of manufacturable large area cells. Since nScrypt's direct printing technology is not yet ready for commercial use because of the need for a high throughput multi-nozzle tool, we decided to focus on commercially viable screen printing technology, which is showing rapid progress. At the start of this chapter we were able to screen print 80 µm lines, as opposed to 100 µm, which raised the screen printed GEN-I PERC cell efficiency from 19.8% to 20.0% (Table 8.1). This is the result of improved Ag pastes and screen designs and materials with finer openings.

**Table 8.1 Evolution of screen printed GEN-I PERC cell efficiency and GEN-II PERC cell efficiency target.**

| | Emitter | Ag Paste | Printing Technology | Voc (mV) | Jsc ($mA/cm^2$) | FF (%) | η (%) |
|---|---|---|---|---|---|---|---|
| GEN-I | Selective (100/50-Ω/sq) | Old (PV16A) | Old (100µm Ag Finger) | 655 | 38.1 | 78.7 | 19.7 |
| GEN-I | Homogeneous (~100-Ω/sq) | New (PV17S) | Improved (80µm Ag Finger) | 656 | 38.3 | 79.5 | 20.0 |
| GEN-II (Target) | Homogeneous (~90-Ω/sq) | New (PV17S) | Improved (60µm Ag Finger) | 670 | 39.5 | 79.7 | 21.0 |

In section 8.1, a low-cost homogeneous emitter with lower surface concentration and optimized anneal conditions will be developed for attaining the target $J_{oe}$ of ~130 $fA/cm^2$ (Figure 8.2). In addition, the passivation quality and thickness of in-situ grown thermal $SiO_2$ and PECVD grown $SiN_x$ AR coating on this new homogeneous emitter will be optimized by reflectance and effective lifetime measurements. In section 8.2, the ion

implantation dose will be optimized to tailor surface concentration, reduce contact loss and achieve higher fill factor. Section 8.3 will describe the third technology enhancement associated with increasing the BSR value above 95%. This will involve ray tracing simulations using the Sunrays optical modeling program to establish the thickness and index for each dielectric layer in the rear stack. Complete PERC cells will be fabricated for experimental validation of the model. In section 8.4, line contact geometries instead of point contacts on the back side will be used to enhance the rear contact quality, manufacturability and throughput. In section 8.5, attempt will be made to improve traditional screen-printed contact technology to further reduce the shadow losses and increase the aspect ratio. In section 8.6, ~21% PERC cells will be fabricated and their light-induced degradation (LID) characteristics will be studied.

## 8.1 Development of Ion-Implanted high Sheet Resistance Homogeneous Emitter for High-Efficiency PERC Cells

### 8.1.1 Modeling to Establish the Joe Requirement for 21% PERC Cell

The 20% screen printed GEN-I PERC cell had a $V_{oc}$ of only 656 mV partly due to a high $J_{oe}$ of ~210 fA/cm$^2$ (Figure 8.1). The roadmap in Figure 8.2 calls for a $V_{oc}$ of ~670 mV and $J_{oe}$ of 133 fA/cm$^2$ for 21% efficiency.

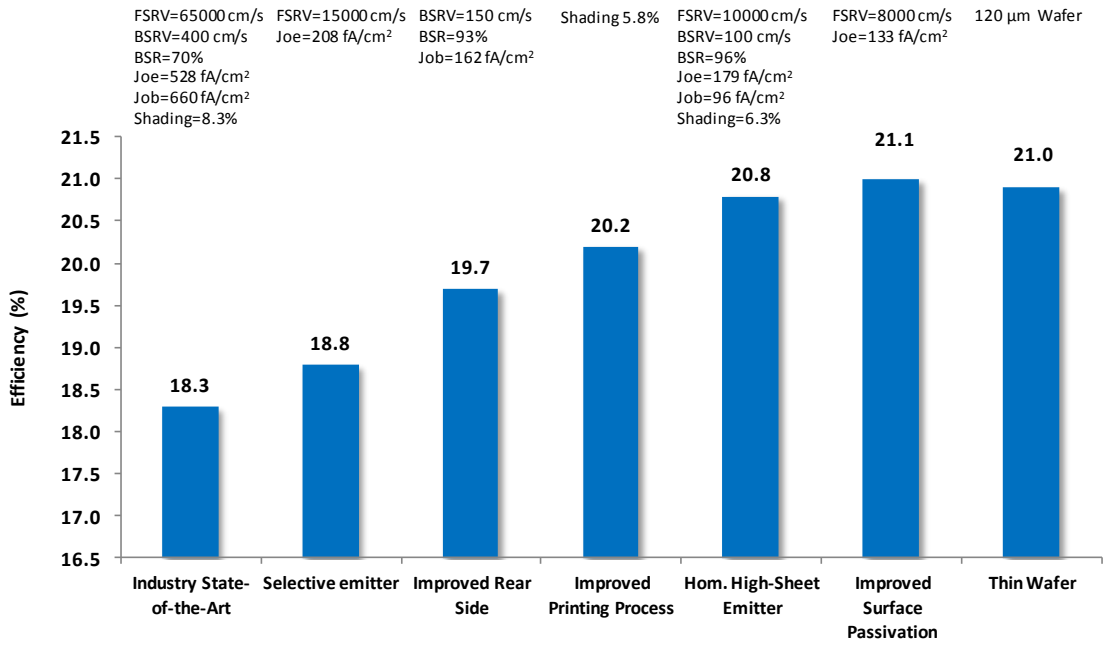



**Figure 8.2 Technology roadmap for achieving ~21% PERC cell.**

Since $J_{oe}$ is composed of $J_{oe\text{-}met}$ under the metal grid and the $J_{oe\text{-}pass}$ in the field region between the metal grid lines, device simultaneous were performed to quantify the two $J_{oe}$ components and establish the target for 21% cell. $J_{oe\text{-}met}$ under the metal contact was calculated by feeding the measured emitter doping profile in PC1D and setting the SRV value to $10^7$ cm/s. Next, the cell was subjected to a forward bias at 0.4 volts in dark

in PC1D to obtain the minority carrier current density $J_p$ at the junction edge on the emitter side, from which the $J_{oe\text{-}met}$ was calculated to be ~1300 fA/cm$^2$ using the equation:

$$J_p = J_{0e} e^{\frac{qV}{kT}} \tag{8.1}$$

This agreed well with the literature [113]. Since front metal fraction (f) was only 7% in the 20% cell, the $J_{oe\text{-}met}$ in the 20% device is calculated to be 1300×0.07 = 91 fA/cm$^2$. Our target is to reduce metal coverage to ~5.5%, which showed reduce $J_{oe\text{-}met}$ to ~66 fA/cm$^2$, leading to a $J_{oe\text{-}pass}$ requirement of 133-66 = 67fA/cm$^2$. Following equation describes the relationship between the $J_{oe}$ components and the metal fraction (*f*):

$$J_{oe-total} = J_{oe-met} \times f + J_{oe-pass} \times (1 - f) \tag{8.2}$$

### 8.1.2 Optimization of Ion Implantation Dose to Achieve the Required $J_{oe\text{-}pass}$ for High Sheet Resistance Emitter

$J_{oe\text{-}pass}$ is a function of emitter bulk recombination as well as surface passivation. $J_{oe\text{-}pass}$ can be determined by a symmetric diffused and passivated test structure shown in Figure 8.3, without making the complete cells.

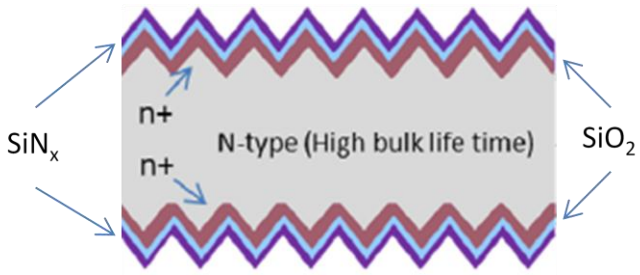



**Figure 8.3 schematic of symmetric test structure used for $J_{oe\text{-}pass}$ measurements.**

This QSS-PC technique is well documented in the literature and requires measuring effective lifetime as a function of injection level in the above structure. The slope of this line gives the $J_{oe\text{-}pass}$ according to the following equation [93]:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{J_{oe}\bar{n}}{qWn_i^2} \tag{8.3}$$

where $\tau_{eff}$ is instantaneous decay time, $\tau_{bulk}$ is the high-level injection lifetime, and $\bar{n}$ is the average photo-excited carrier density in the sample.

In order to explore different emitters, implanted doses was varied in the range of $1\times10^{15}$ to $7\times10^{15}$ $cm^{-2}$ and implant anneal was performed at 840˚C for 50 min, including 30 min anneal in $O_2$ followed by 30 min in $N_2$. This resulted in oxide passivated emitter on both sides of the wafer. A 500Å PECVD nitride coating was deposited at 450˚C on both sides followed by a simulated contact firing cycle at 800˚C, identical to what the emitter sees during the cell fabrication. After this QSS-PC tool was used to measure $J_{oe\text{-}pass}$ of various emitters with the objective of achieving $J_{oe\text{-}pass}$ value of $\leq$ 67 $fA/cm^2$. $J_{oe\text{-}pass}$ values were compared with the implanted selective emitter and the $POCl_3$ emitters in the previous emitter. Figure 8.4 shows that $J_{oe\text{-}pass}$ of $\leq$ 67 $fA/cm^2$ can be achieved with 100 Ω/sq homogeneous emitter implant after contact firing cycle with the implant dose of $2.7\times10^{15}$ $cm^{-2}$. All other emitters do not qualify for 21% cell because the $1\times10^{15}$ $cm^{-2}$ dose gave ~200 Ω/sq.emitter wich is diffucult to contact.

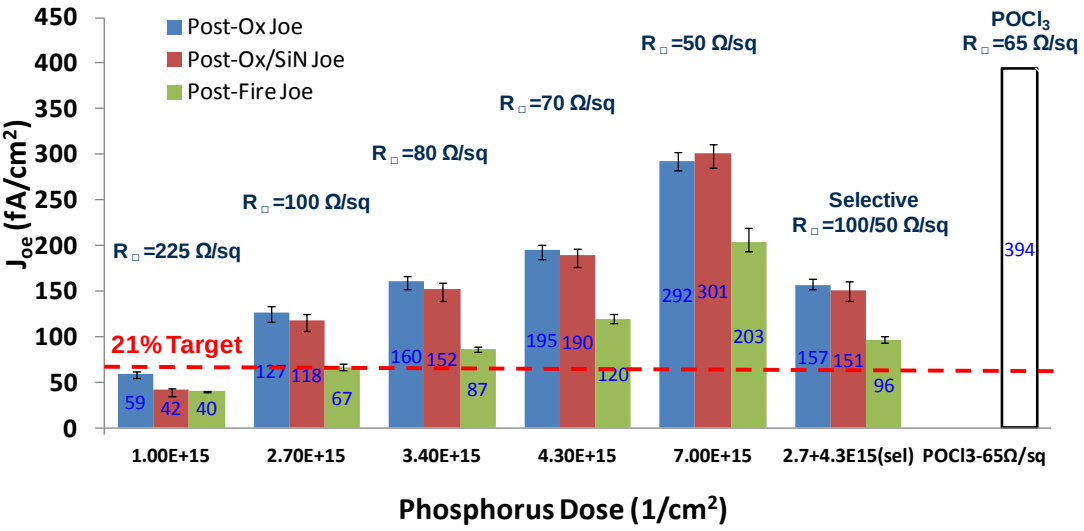



**Figure 8.4 $J_{oe\text{-}pass}$ comparison of different ion implanted emitters at different process steps. The dashed lines show the target $J_{oe\text{-}pass}$ value (67 fA/cm$^2$) for achieving a ~21% cell with local Al-BSF.**

Therefore, cell data in Table 8.2 shows that 100 Ω/sq emitter cells also gave very high series resistance (~2 Ω-cm$^2$) resulting in a very poor FF (~0.71) and cell efficiency (~17.3%). This shows there are additional challenges in optimizing homogeneous emitter which can satisfy $J_{oe}$ and FF requirements simultaneously.

**Table 8.2 Light I-V data for the initial study of ion-implanted homogeneous emitter (~100 Ω/sq) cell.**

| $V_{OC}$ (mV) | $J_{SC}$ (mA/cm$^2$) | FF (%) | η (%) | $R_s$ (Ω-cm$^2$) |
|---|---|---|---|---|
| 649 | 37.6 | 71.0 | 17.3 | 2.17 |
| 647 | 37.5 | 72.4 | 17.6 | 1.84 |
| 647 | 37.5 | 70.7 | 17.2 | 2.27 |
| 648 | 37.6 | 71.2 | 17.3 | 2.20 |
| 650 | 37.8 | 69.9 | 17.2 | 2.46 |

### 8.1.3 Optimization of Ion Implantation Anneal for Homogeneous Emitter to Achieve Low $J_{oe\text{-}pass}$ and High FF

Besides the dose, implantation anneal also plays an important role in controlling the profile and surface concentration. Therefore, in this study we fixed the dose at $2.6\times10^{15}$ $cm^{-2}$, and varied the DCE oxidation time from 5 to 60 min at 855˚C followed by 10 min anneal in $N_2$ ambient. Again, 500Å PECVD $SiN_x$ coating was deposited on both sides followed by simulated contact firing to prepare the symmetric test structure (Figure 8.3). Figure 8.5 shows that $J_{oe\text{-}pass}$ decreases as the DCE oxidation time increases and the $J_{oe\text{-}pass}$ value of $\leq$ 67 $fA/cm^2$ were achieved $\geq$ 20 min oxidation after the contact firing cycle. Some unimplanted planar bare Si wafers were also kept in the furnace during the anneal to determine the oxide thickness. Figure 8.6 shows the corresponding oxide thickness which increased from 80Å to 140Å on undiffused bare Si wafer when the oxidation time was increased from 20 to 60 min. It is important to recognize that oxide grows almost three times faster on $n^+$ surface compared to bare Si. Therefore, oxide thickness on the textured diffused surface was expected to be 240 to 420Å for 20 and 60 min oxidations. It is also known that once the oxide thickness starts to exceed 200Å, it is difficult to optimize the nitride coating thickness to avoid anti-reflection losses. This narrowed the choice to 20 min oxidation time.

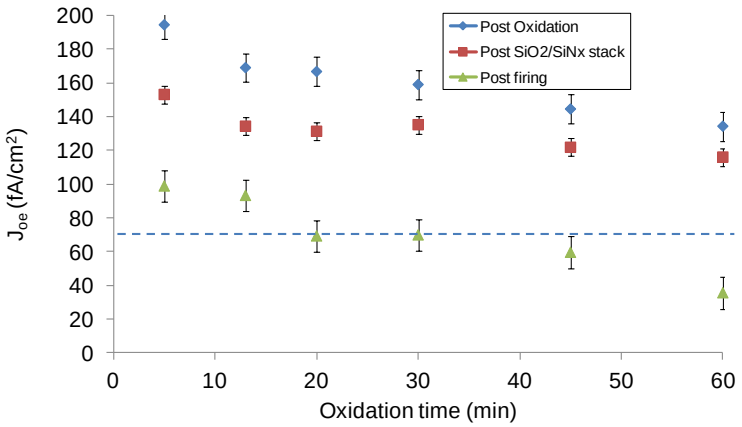



**Figure 8.5 Measured $J_{oe}$ of different oxidation time after different cell process steps. The dashed line shows the target $J_{oe,pass}$ value (67 fA/cm$^2$) for achieving ~21% PERC cell.**

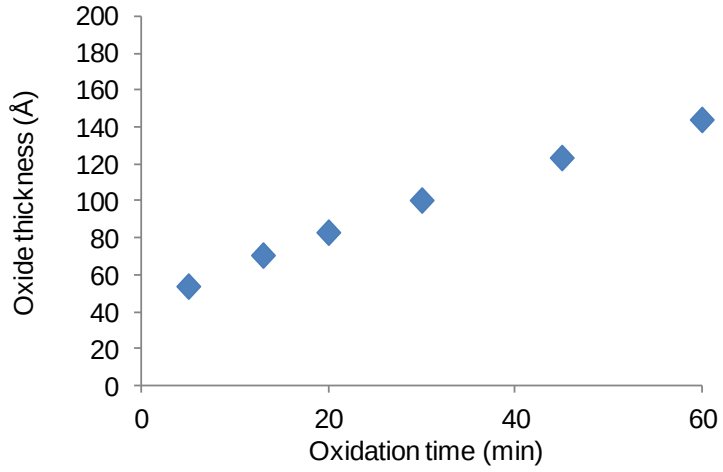



**Figure 8.6 Oxide thicknesses as a function of oxidation time (5-60 minutes).**

After satisfying the $J_{oe\text{-}pass}$ and optical loss requirements, the next challenge was to ensure that the doping profile, sheet resistance and surface concentration were acceptable for contact resistance and FF requirements. Therefore, SIMS and SRP measurements were performed to study the doping profiles (Figure 8.7). It is interesting to note that SIMS and SRP profiles matched very well for all the six anneal times (5-60 min),

indicating that the emitters are properly annealed and there is not much inactive P near the surface which often increases the emitter recombination. As expected increased annealing time lowered the surface concentration and drove the junction deeper. Note that surface concentration ranged from 1 to 2 $\times 10^{20}$ $cm^{-3}$ with 20 min oxidation resulting in surface concentration of ~$1.97\times 10^{20}$ $cm^{-3}$. The sheet resistance increased from 92 to 95 when oxidation increased from 5 to 60 min.

Next, we experimented with several emerging Ag pastes in collaboration with our industry partners and found some pastes that can make good contact to 1.5 to $2\times 10^{20}$ $cm^{-3}$ surface concentration. After developing the ~100 Ω/sq emitter that satisfies the requirement for $J_{oe\text{-}pass}$, sheet resistance, surface concentration and screen printed contact, the next step was to ensure that the 20 min oxidation used for this emitter does not increase the front surface reflectance and also satisfies the BSRV requirement of < 100 cm/s. This is discussed in the following section.

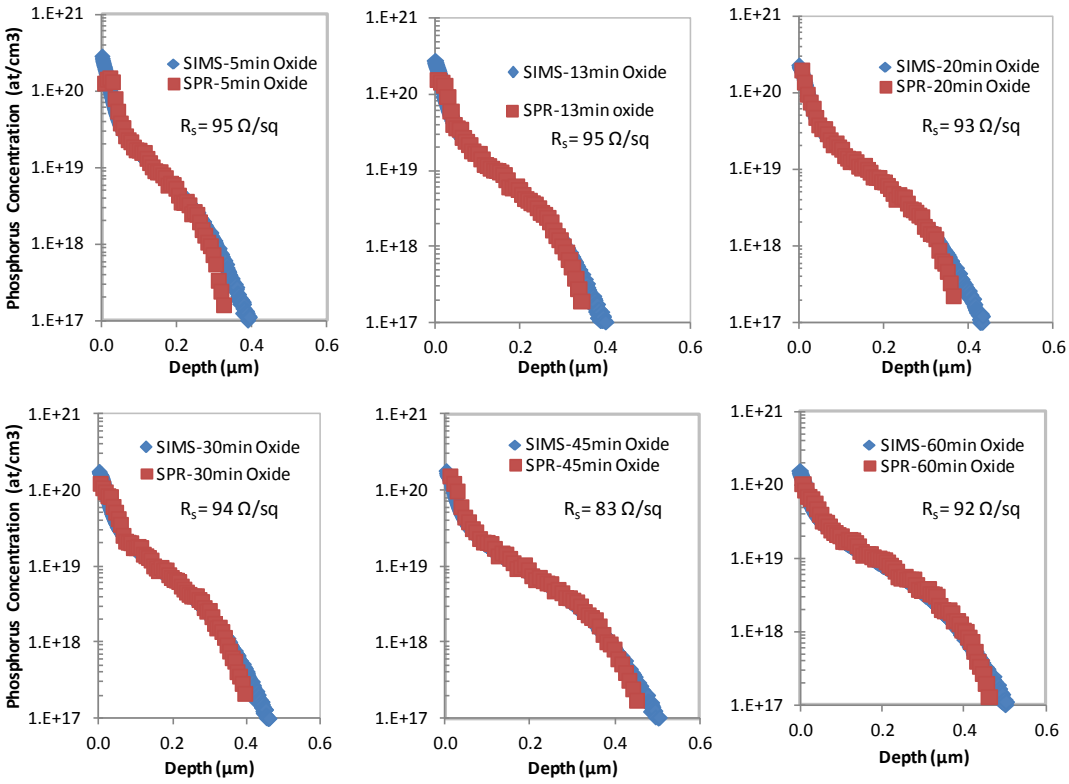



**Figure 8.7 SIMS and SRP profiles for different oxidation conditions.**

### 8.1.4 Back Surface Passivation Quality for Different Anneals

In order to quantify the quality and thermal stability of the oxide layers, symmetric test structure were fabricated to measure effective lifetime (Figure 8.8). Double-side textured wafers were planarized by KOH etching for 15 minutes at 80˚C followed by thermal oxidation (5-60 minutes) at 855˚C to passivate both sides of the wafers. The oxide layers were then capped with a 450 Å thick PECVD $SiN_x$ layer and subjected to a high temperature contact firing cycle to simulate the cell fabrication sequence without metallization.

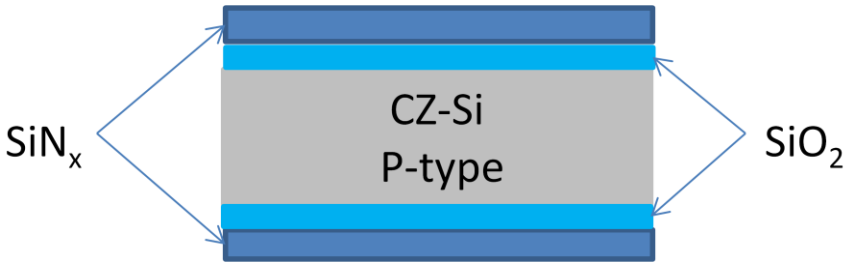



**Figure 8.8 Schematic of symmetric test structure for lifetime measurements.**

Figure 8.9 shows the surface recombination velocity of different oxidation after simulated firing process step. The surface recombination velocity $S_{eff}$ was calculated using the equation:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{bulk}} + \frac{2S_{eff}}{W} \qquad (8.4)$$

where $\tau_{eff}$ and $\tau_{bulk}$ are the effective and bulk lifetime, measured by QSS-PC method and $W$ is the wafer thickness. The $S_{eff}$ value for 5 minute oxidation was 135 cm/s which reduced to 79 cm/s after the 20 minute oxidation and then decreased slightly to 75 cm/s when the oxidation time was increases to 60 minutes. This was found to be the result of lower oxide charge ($Q_{ox}$), and interface state density ($D_{it}$) in thicker oxide (Figure 8.10). Based on our roadmap in Chapter 3, the required BSRV for ~21% PERC cell is < 100

cm/s. Therefore, the 20 min oxidation which gave a BSRV of 79 cm/s, also satisfies the BSRV requirement.

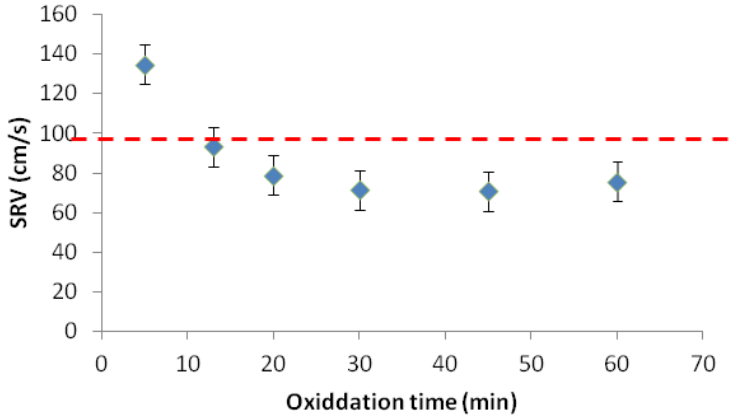



**Figure 8.9 Change in surface recombination velocity of different oxidation.**

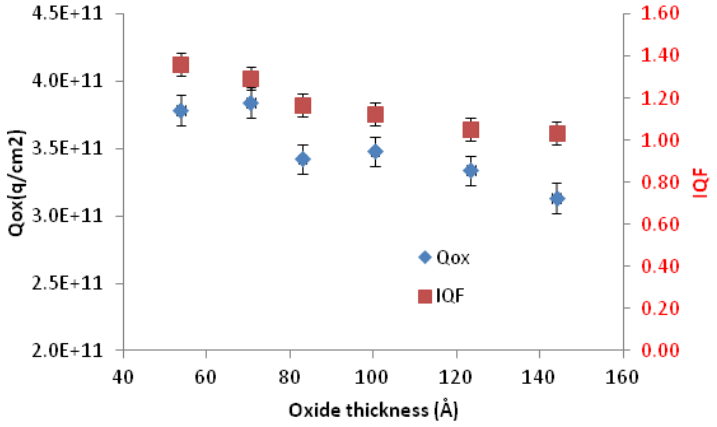



**Figure 8.10 Fixed oxide charge and interface quality factor as a function of rear oxide thickness.**

### 8.1.5 Fabrication of High-Efficiency Screen-Printed PERC Cells with Optimized Homogeneous Emitter

After establishing the process which satisfies most of the requirements for a high sheet resistance homogeneous emitter cell ($J_{oe\text{-}pass}$, BSRV, contact $N_s$, and reflection), complete PERC cells were fabricated to validate the benefit of this emitter on cell efficiency. Process sequence was similar to the one described in Section 6.2, except the homogeneous emitter and line contacts (instead of vias) on the back. Six different oxides (Figure 8.7) were grown and by varying the oxidation time capped with PECVD $SiN_x$ film. The PECVD anti-reflection coating thickness was adjusted for each oxidation time (Table 8.3) to tune antireflective properties by minimize reflection losses. This was done with the help of Sunrays optical modeling program which optimizes $SiN_x$ thickness for a given oxide thickness. Figure 8.10 shows the cell data including $V_{oc}$, $J_{sc}$, and FF for all six oxidation times (5-60 min). Note that $V_{oc}$ increases rapidly by ~15 mV when oxidation time is increased from 5 to 20 min and then it levels off. This entirely consistent with the $J_{oe}$ and BSRV finings which showed a rapid decrease initially followed by slow change (Figure 8.5 and Figure 8.9). $J_{sc}$ also increases initially but then it starts to drop after 10 min oxidation. This is because front and back passivation improves with oxidation time but after 10 min oxidation front oxide increases too thick to prevent reflective losses. The measured reflectance in Figure 8.12 shows that longer oxidation time has higher short wavelength reflectance in the range of 300 to 500 nm. Figure 8.13 shows that the cells with thicker oxide gave lower fill factor (FF), which is attributed to lower surface concentration for longer oxidation. On the other hand, shorter oxidation time tends to give lower FF due to higher n-factor (>1.2).

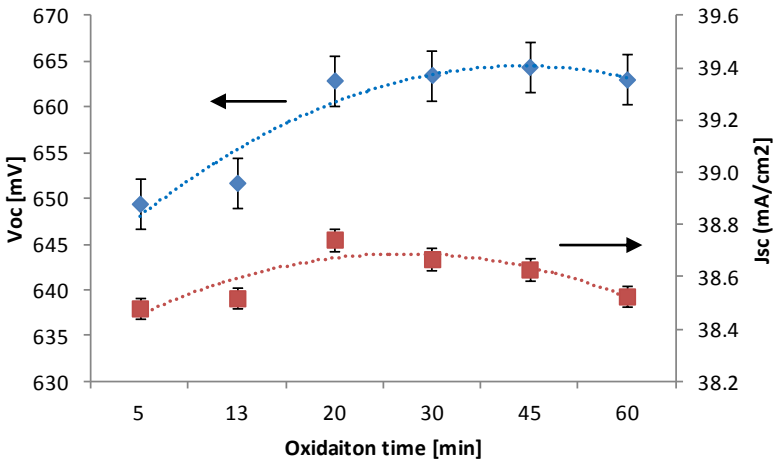



**Figure 8.11 Open-circuit voltage ($V_{oc}$) and short-circuit current density ($J_{sc}$) as a function of different oxidation times.**

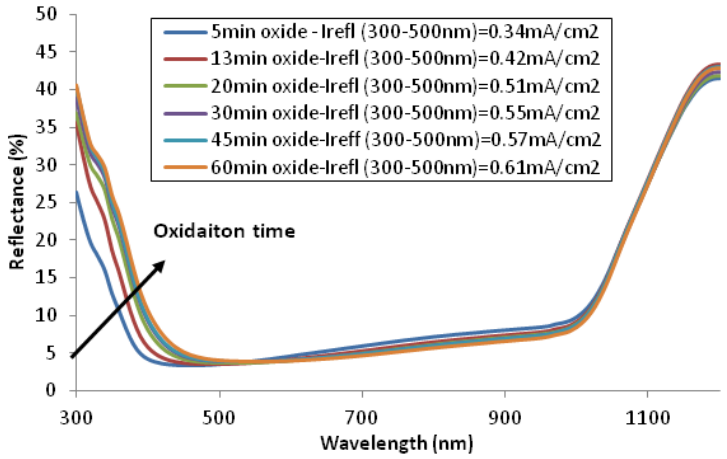



**Figure 8.12 Reflectance of PERC cell as a function of different oxidation time.**

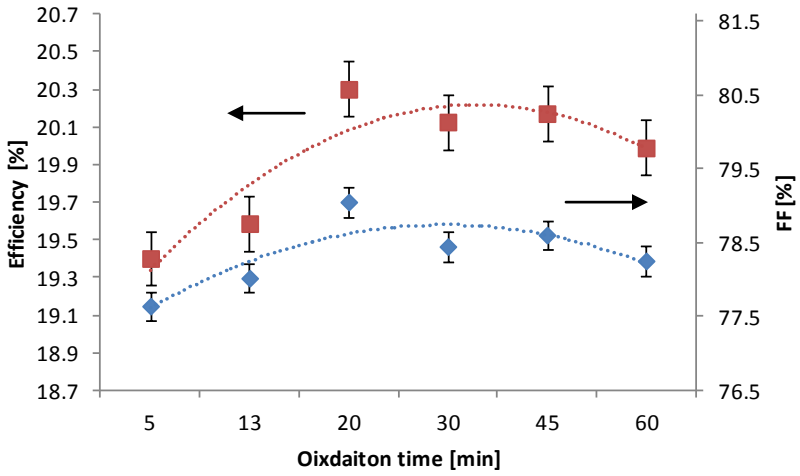



**Figure 8.13 Cell efficiency (η) and fill factor (FF) as a function of different oxidation times.**

Table 8.3 also shows the data for the 20% efficient GEN-I screen printed in addition to the cell parameters for different oxidation times. It is clear that ion implanted homogeneous emitter developed in this study gave ~0.4% increase in PERC cell efficiency with maximum efficiency of 20.4% because of improved $J_{oe\text{-}pass}$, and BSRV without sacrificing FF and optical properties. $V_{oc}$ increased by ~8 mV and $J_{sc}$ improved by ~0.5 mA/cm$^2$. However, the FF dropped appreciably below 0.795, which needs to be improved further to obtain ~21% efficiency.

**Table 8.3 Average (10 cells per each group) and the best light I-V parameters of the ion-implanted homogeneous emitter PERC cells.**

| Oxidation (min) | Oxide/Nitride Thickness (Å) | | $V_{oc}$ (mV) | $J_{sc}$ (mA/cm$^2$) | FF (%) | η (%) |
|---|---|---|---|---|---|---|
| 5 | 160/550 | average | 649 | 38.5 | 77.6 | 19.4 |
| | | best | 651 | 38.6 | 78.2 | 19.6 |
| 13 | 210/520 | average | 652 | 38.5 | 78.0 | 19.6 |
| | | best | 653 | 38.6 | 78.3 | 19.7 |
| 20 | 250/450 | average | 663 | 38.7 | 79.1 | 20.3 |
| | | best | 664 | 38.8 | 79.0 | 20.4 |
| 30 | 300/430 | average | 664 | 38.7 | 78.5 | 20.1 |
| | | best | 664 | 38.8 | 79.0 | 20.3 |
| 45 | 370/380 | average | 664 | 38.6 | 78.6 | 20.2 |
| | | best | 665 | 38.6 | 78.9 | 20.2 |
| 60 | 430/310 | average | 663 | 38.5 | 78.3 | 20.0 |
| | | best | 664 | 38.5 | 78.7 | 20.1 |
| GEN-I Screen-Printed Cell | 300/430 | Reference | 656 | 38.3 | 79.5 | 20.0 |

## 8.2 Optimization of Ion Implantation Dose for Achieving High Fill Factor

In the previous section, an optimized high-quality ion implanted homogeneous emitter was developed with excellent surface passivation in a single high-temperature step. This involved a lightly doped P implantation ($2.6\times10^{15}$ $cm^{-2}$) and an optimized annealing recipe with 20 min oxidation at 855˚C. This homogeneous emitter resulted in $J_{oe}$ of ~67 $fA/cm^2$ (without contacts) and enabled a high $V_{oc}$ of 664 mV and cell efficiency of 20.4%. This ~100Ω/sq lightly doped emitter was contacted with the new screen printed silver paste (DuPont PV17S) and optimized firing recipe which allowed good ohmic contact to this emitter with a surface concentration of $1.97\times10^{20}$ $cm^{-3}$. However, the contact resistance was still somewhat high, resulting in FF of ≤ 0.790. According to technology roadmap in Chapter 4, 21% cell requires a FF of ~0.800. Therefore, an effort was made in this section to boost FF by raising the surface concentration, without appreciably sacrificing $J_{oe}$, $V_{oc}$ and $J_{sc}$. Six different phosphorus doses in the range of 2 to $3.2\times10^{15}$ $cm^{-2}$ were examined to fine tune the homogeneous emitter. Rest of the cell process sequence remained unchanged (Section 8.1) including the 855˚C annealing recipes, which involved 20 min oxidation followed by 10 min $N_2$ anneal.

Figure 8.14 and Figure 8.15 shows the result of increasing the implant dose from $2.0\times10^{15}$ to $3.2\times10^{15}$ $cm^{-2}$. As the phosphorus dose increases, both $V_{oc}$ and $J_{sc}$ begin to decrease because emitter recombination increases due to heavy doping effects and also the junction deepens. However, FF rises to about 0.800 due to high emitter surface concentration and saturates after a close of $2.8\times10^{15}$ $cm^{-2}$. This is supported by the measured lower series resistance at higher phosphorus dose (Figure 8.16). Figure 8.15 and Table 8.4 show that implant dose of $2.8\times10^{15}$ $cm^{-2}$ produced the best cell efficiency of 20.5% with a FF of 0.798.

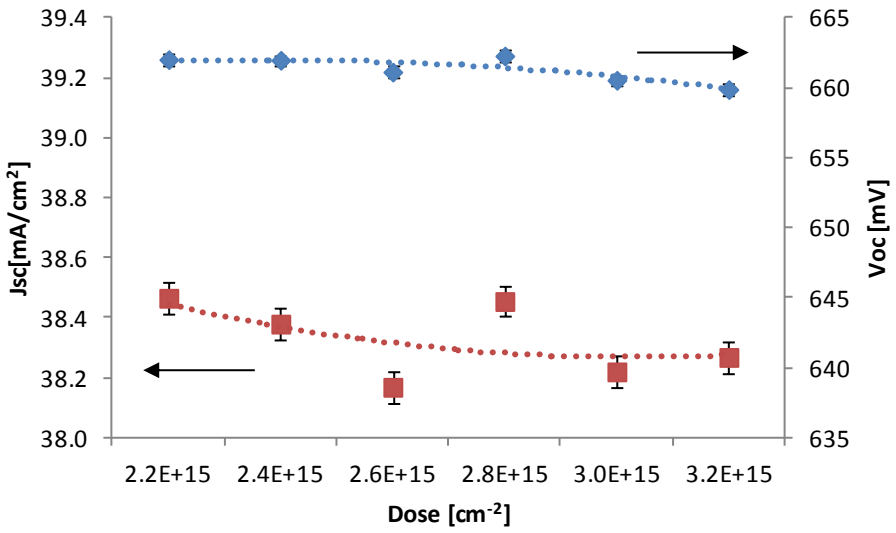



**Figure 8.14 $V_{oc}$ and $J_{sc}$ as a function of different phosphorous does.**

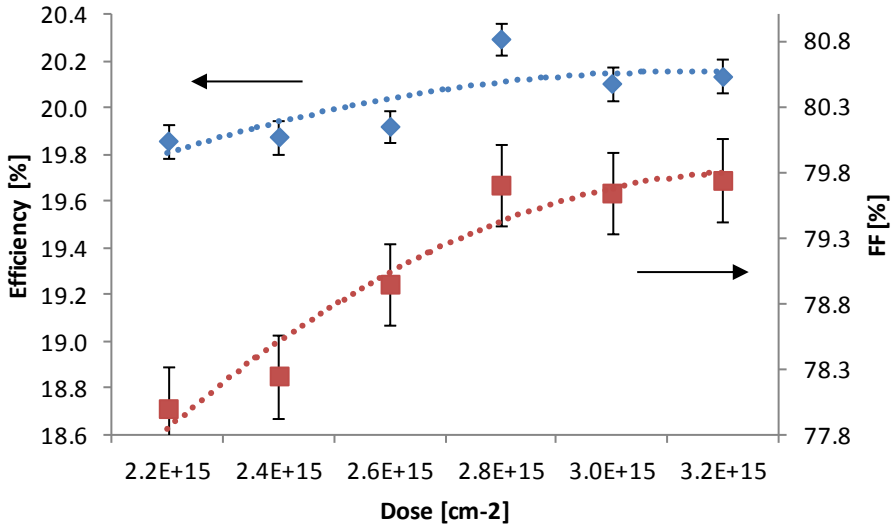



**Figure 8.15 Efficiency and FF as a function of phosphorous dose.**

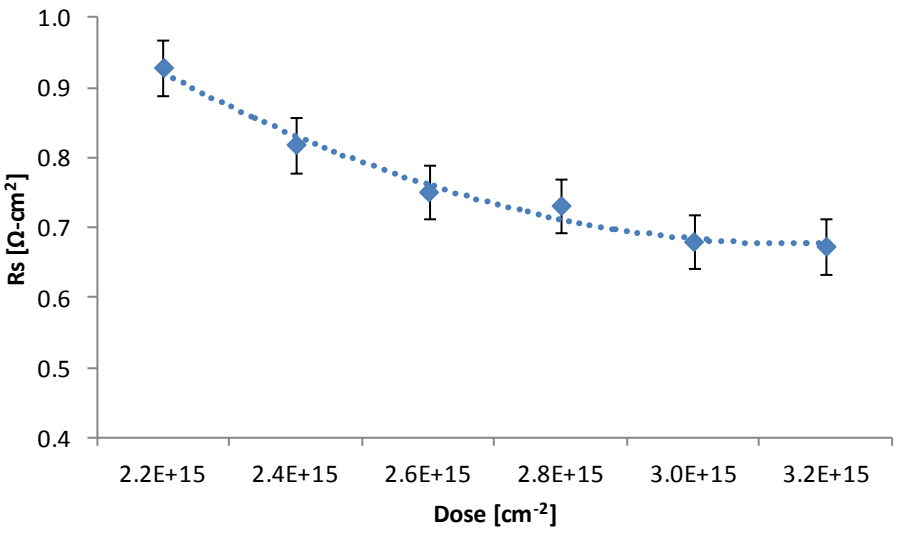



**Figure 8.16 Series resistance ($R_s$) a function of different phosphorous does.**

**Table 8.4 Average (10 wafers per each group) and the best light I-V parameters of the ion-implanted homogeneous emitter PERC cells.**

| Implant Dose ($P/cm^2$) | | $V_{oc}$ (mV) | $J_{sc}$ ($mA/cm^2$) | FF (%) | η (%) |
|---|---|---|---|---|---|
| $2.2\times10^{15}$ | average | 662 | 38.5 | 78.0 | 19.9 |
| | best | 663 | 38.5 | 78.5 | 20.0 |
| $2.4\times10^{15}$ | average | 662 | 38.4 | 78.2 | 19.9 |
| | best | 662 | 38.5 | 78.4 | 20.0 |
| $2.6\times10^{15}$ | average | 661 | 38.2 | 78.9 | 19.9 |
| | best | 660 | 38.3 | 79.3 | 20.0 |
| $2.8\times10^{15}$ | average | 662 | 38.5 | 79.7 | 20.3 |
| | best | 663 | 38.7 | 79.8 | 20.5 |
| $3.0\times10^{15}$ | average | 661 | 38.2 | 79.6 | 20.1 |
| | best | 661 | 38.2 | 80.0 | 20.2 |
| $3.2\times10^{15}$ | average | 660 | 38.3 | 79.7 | 20.1 |
| | best | 661 | 38.4 | 80.0 | 20.3 |

Internal quantum efficiency (IQE) and reflectance measurements (Figure 8.17) were performed on a 20.4% efficient PERC cell fabricated with a $2.8\times10^{15}$ $cm^{-2}$ dose. PC1D modeling was used to match of the experimental I-V, IQE, reflectance data to extract BSRV and BSR values. This analysis revealed a BSR value of 93%, and an

excellent BSRV and FSRV values of 100 cm/s and 10,000 cm/s, respectively. Both experimental and model IQE data agreed very well in Figure 8.17, using a $Q_{ox}$ value of $2\times10^{11}$ in the PC1D for the dielectric. Our technology roadmap in Chapter 4 showed that ~21% efficiency requires a BSR of ≥ 95%. Therefore, in the next section we will investigate back surface reflector design with the aim to boost the BSR to ≥ 95% using the low-cost $SiO_2/SiN_x$ dielectric stack.

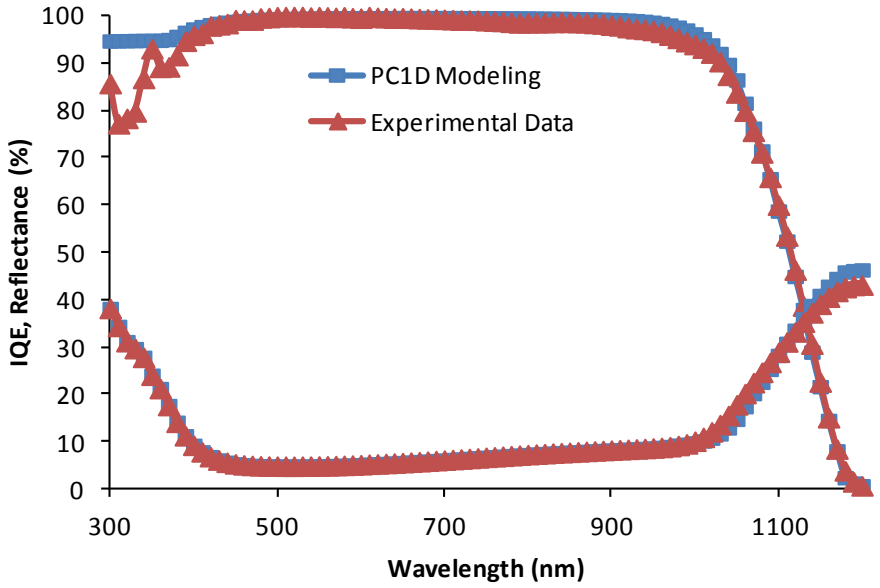



**Figure 8.17 IQE and reflectance of a 20.4% PERC cell with PC1D modeling outputs.**

## 8.3 Understanding and Optimization Front and Back Optical Properties to Enhance the Efficiency of the PERC Cells

In the previous two sections, a low-dose homogeneous emitter was developed and optimized to produce 20.5% PERC cell with high $V_{oc}$ (> 664 mV), $J_{sc}$ (> 38.7 mA/cm$^2$) and FF (~0.798). This was achieved by reducing emitter and back surface recombination, the front surface recombination velocity (FSRV) of 10,000 cm/s and back surface recombination velocity of 100 cm/s (BSRV), which can attain 21% efficiency. However, the back surface reflectance of 93% which is good but not good enough for 21% cell. Therefore, this section will focuses on driving the back surface reflectance to the target of 96%.

As discussed in Chapter 4, high quality anti-reflection coatings (ARC) in conjunction with excellent back surface reflector (BSR) is important for minimizing the optical loss. In the laboratory PERC cells in the literature, photolithography defined inverted pyramids with a double-layer ARC ($ZnS/MgF_2$) are used to minimize the front surface reflection. On the back side, planarized surface and a thick thermally-grown $SiO_2$ (105 nm) with evaporatored Al is used to enhance the back surface reflectance. However, such ARC and BSR processes are too complex and expensive for commercial cells. Therefore, the objective of this task is to develop a low-cost manufacturable dielectric stack with screen printed metal to achieve high rear internal reflectance (≥ 95%) without sacrificing the surface recombination velocity.

To accomplish the above goal, detailed optical modeling was performed using a ray tracing program, called Sunrays, to gain quantitative understanding and establish the required thickness and index for each dielectric layer in the oxide/nitride stack to reduce front reflection in conjunction with high rear internal reflectance. Various dielectric stacks were then grown and characterized to validate the results of the optical modeling.

Implied $V_{oc}$ measurements using QSS-PC were also performed to ensure that the passivation quality is maintained for the new stacks.

### 8.3.1 Optical Modeling to Optimize Anti-reflection Coating for High-Efficiency PERC Cell

In Chapter 6, we showed that a thicker back oxide (~90Å) was important to achieve high quality surface passivation. However, thicker back oxide results in much thicker front oxide because oxide grows almost three times faster on heavily doped $n^+$ Si compared to p-Si. This could result in ~250 Å oxide on the front and degrade $J_{sc}$ if nitride thickness is not optimized. Therefore, Sunrays program was used to optimize the thickness and index of front PECVD $SiN_x$ to retain the full benefit of high quality rear surface passivation.

Table 8.5 summarizes structure and optical parameters of each layer for optical simulations. The simulated device had a front surface with an upright pyramid texture coated with a dielectric stack of 250 Å $SiO_2$ (n = 1.46) and a $SiN_x$ with index of n = 2.05 with variable thickness. The optimum $SiN_x$ thickness was determined numerically by the optical modeling using minimum front surface reflection as the criteria. The back surface of the modeled structure was planar with a stack of 80 Å $SiO_2$ (n = 1.46) and 600 Å $SiN_x$ (n = 2.05) and Aluminum for back reflector. Note that the back $SiN_x$ thickness was not optimized in this simulation, but will be optimized in the next section after the AR coating optimization.

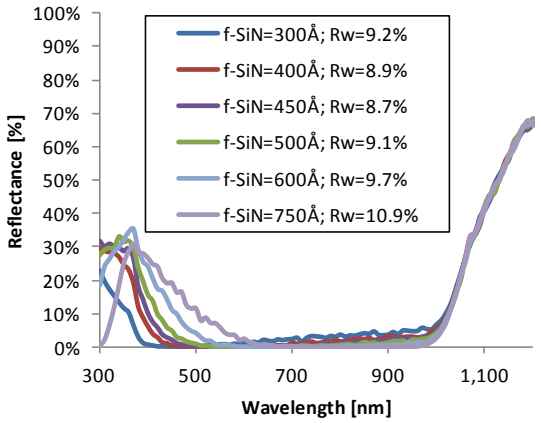
**Table 8.5 Sunrays simulation parameters for determining optimized $SiN_x$ thickness for the PERC cell.**

| | | |
|---|---|---|
| Texturing | Structure | Upright pyramid |
| | Width | 5 μm |
| | Depth | 3.535 μm |
| Material/Layer | Front | Air (n=1) |
| | Encapsulant | Air (n=1) |
| | Texture | Silicon (n=3.8) |
| | Substrate | Silicon (n=3.8) |
| | Back Metal | Aluminum |
| Antireflection coating | Front/encapsulant | Air (n=1) |
| | Encapsulant/texture-Top | Air (n=1) |
| | Encapsulant/texture-Middle | SiN (2.05); variable |
| | Encapsulant/texture-Bottom | $SiO_2$ (1.46); 250Å |
| | Back surface reflector-Top | $SiO_2$ (1.46); 80Å |
| | Back surface reflector-Middle | SiN (2.05); variable |
| | Back surface reflector-Bottom | Aluminum |
| Illumination | | Normal |
| Spectrum | | AM1.5G |
| | Polarization | Unpolarized |

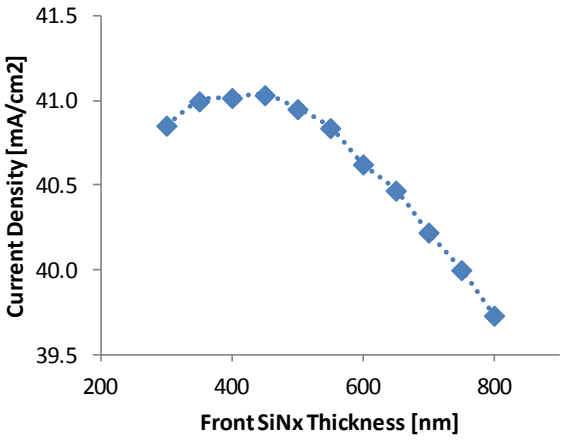
Figure 8.18 (a) shows the simulated reflectance curves and the integrated total reflectance ($R_w$) for six different $SiN_x$ thicknesses in the range of 300 to 750 Å on top of the 250 Å oxide. Figure 8.18 (b) shows the corresponding short-circuit current density assuming 100% collection efficiency. The average weighted reflectance, $R_w$, accounts for the reflectance $R(\lambda)$ and photon flux $F(\lambda)$ at each wavelength in the AM1.5G spectrum. The $R_w$ is essentially the reflected photocurrent divided by the total available photocurrent and can be expressed as:

$$R_w = \frac{\int_{\lambda_1}^{\lambda_2} F(\lambda)R(\lambda)d\lambda}{\int_{\lambda_1}^{\lambda_2} F(\lambda)d\lambda} \tag{8.5}$$

The $R_w$ calculations (Figure 8.18 (a)) clearly show that 450 Å $SiN_x$ film in conjunction with the 250Å thermally grown oxide gives the minimum average weighted reflectance of 8.7% and highest short-circuit current density of 40.02 mA/cm$^2$ (Figure 8.18 (b)).




(a)




(b)

**Figure 8.18 (a) Simulated reflectance and calculated average weighted reflectance ($R_w$) for six different SiNx AR coatings. (b) Calculated short-circuit current density for different $SiN_x$ AR coatings.**

To gain a better understanding of the impact of the oxide thickness on the front surface reflection loss, we also simulated various AR coatings with 100 Å and 250 Å oxides, capped with SiNx films in the range of 300 Å to 900 Å. $SiN_x$ index was also raised from 2.0 to 2.1. Figure 8.19 shows that the impact of refractive index of $SiN_x$ in the range of 2.0 to 2.1 has negligible effect on reflection loss. As expected higher $SiO_2$ thickness requires thinner $SiN_x$ for minimum loss. The good news is that even with the 250 Å thick oxide, minimum reflective current density can made nearly equivalent to the 100 Å oxide provided the $SiN_x$ thickness is reduced from 600 to 450 Å. Without this thickness optimization, $J_{sc}$ would decrease by ~0.5 $mA/cm^2$ for the 250 Å oxide.

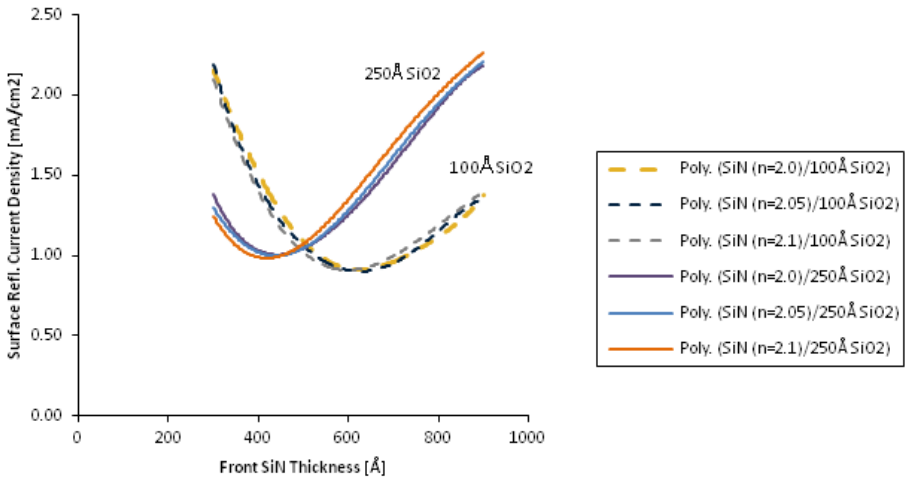



**Figure 8.19 Calculated surface reflected current density as a function of the thickness of $SiO_2$ and $SiN_x$ films on a upright textured surface with normally incident light. Reflective index of $SiN_x$ films varies in the range of 2.0 to 2.1.**

### 8.3.2 Experimental Validation of Optical Modeling

To validate the results of optical modeling, test samples were fabricated with the various stacks of SiO2 (n = 1.46) and SiN (n = 2.05). The quality of the AR coatings was characterized by measuring total reflectance curves. In addition, the average weighted reflectance was also calculated for each AR coating in the wavelength range of 400 to 700 nm (Figure 8.20). To obtain different oxide thicknesses, three samples with the original 250Å thick thermally grown $SiO_2$ were etched back in 10% HF for 15, 20, 30 seconds to obtain 175 Å, 150 Å and 100 Å oxides. The thickness of PECVD $SiN_x$ was adjusted for the thinner oxides to achieve best antireflective properties. Figure 8.20 shows the measured reflectance curves and their corresponding $R_w$ values. The results confirmed that for the 250 Å oxide, 450 Å $SiN_x$ gave the lowest $R_w$ (2.5%). However, it also indicates that a thinner oxide (~100 Å) in conjunction with the optimized $SiN_x$ thickness of 635 Å could gave a slightly lower $R_w$ (2.2%). Since 80 Å thickness is necessary on the back, which gives 250 Å oxide on the front, the only way to regain this 0.3% loss in $R_w$ is by controlled oxide etch back to ~100 Å, which may not be practical and cost effective for mass production.

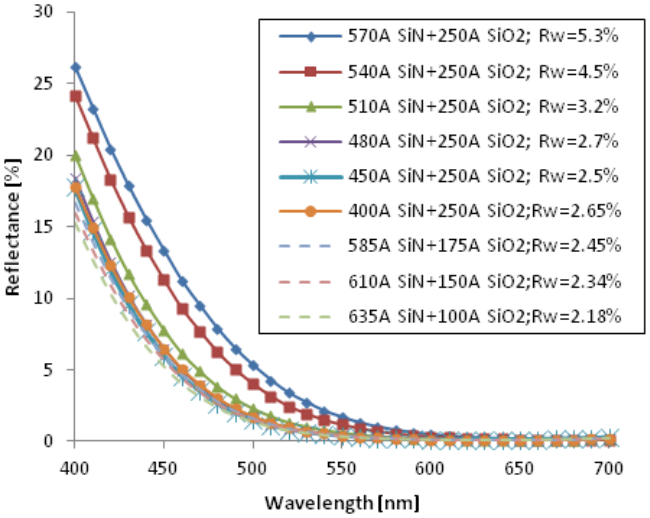



**Figure 8.20 Comparison of measured reflection and average weighted reflectance ($R_w$) of the samples with different $SiO_2/SiN_x$ AR coating stacks on the front surface.**

### 8.3.3 Optical Modeling and Optimization of the Back Surface Reflector for the High Efficiency PERC Cell

In addition to optimizing the AR coating, the rear surface reflector also needsto be optimized because it impacts $J_{sc}$ by contributing to light trapping. Current state-of-the-art industrial solar cells have full area Al-reflector in contact with silicon, which provides a modest back surface reflectance (BSR) of ~70% due to the absorption of long wavelength photons in the screen-printed aluminum. However, with the PERC structure, which utilizes dielectric passivation and local back contacts, the BSR can be significantly improved to above 90% [61]. Various types of back surface reflectors have been proposed in the literature to enhance reflectance, including textured dielectric, dielectric/metal stacks, ordered gratings, reflective pigment-loaded dielectrics, white paint reflector, brushed-on Ag colloid [114-119]. Although these BSR technologies have superior diffuse reflectance properties, but some of them result in inferior passivation, poor conductivity, or both. Moreover, their complex fabrication process results in higher manufacturing cost which does not meet our criteria of low-cost manufacturable technology.

This section focuses on exploring a low-cost dielectric stack composed of thin thermally grown $SiO_2$ and PECVD $SiN_x$ that can simultaneously achieve high quality surface passivation and high rear internal reflectance ($\geq$ 95%). To accomplish this task, optical simulations were performed using Sunrays to establish the requirements thickness and index for each dielectric layer. The simulated cell structure and optical parameters are similar to the AR coating modeling in Table 8.5 except the criteria is to maximize the BSR value. The device has an upright-textured front surface with the optimized 250 Å /450 Å Oxide/SiN AR coating (established in the previous study), a planar back with a dielectric stack composed of 80 Å $SiO_2$ (n = 1.46) and a 2.05 index $SiN_x$ layer of variable thickness. Aluminum layer on top of the dielectric stack was used to enhance reflectance.

Figure 8.21 shows the simulated reflectance curves and the corresponding back surface reflectance ($R_b$) value. The results show that a 1600 Å thick $SiN_x$ layer can provide 97.8% BSR. However, it takes longer process time may lead to wafer bowing due to the thermal expansion coefficient mismatch between Si and $SiN_x$ film.

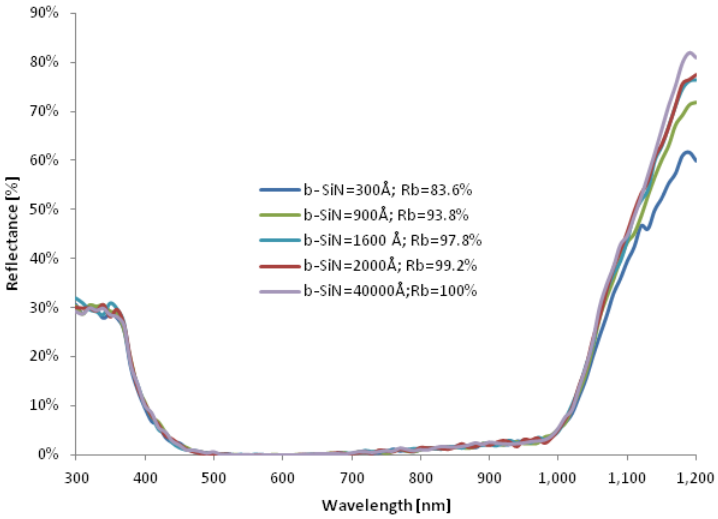



**Figure 8.21 Simulated reflectance curves and their corresponding back surface reflectance ($R_b$) values for five dielectric stacks consisting of a 80 Å $SiO_2$ (n = 1.46) plus a $SiN_x$ layer (n = 2.05) of variable thickness.**

### 8.3.4 Experimental Validation of Optical Modeling of BSR as a Function of $SiN_x$ Thickness

To validate the optical modeling, complete PERC cells were fabricated with 1600 Å and 2000 Å thick $SiN_x$ on top of the 80 Å oxide on the back. All other cell process parameters were kept the same. The cell data in Table 8.6 shows that the thicker $SiN_x$ resulted in ~0.1% higher efficiency. Highest efficiency of 20.6% was achieved with 2000 Å thick $SiN_x$ layer on top of ~80 Å oxide. These two stacks gave similar open-circuit voltage of 666 mV and FF of 79.4%, but the stack with 2000 Å $SiN_x$ gave 0.2 mA/cm$^2$

higher short-circuit current density. PC1D device modeling program was used to calculate the BSR ($R_b$) value by matching the calculated and measured escaped reflectance above $\lambda > 1000$ nm (Figure 8.22). This analysis gave a BSR value of ~95% for the cell with 1600 Å thick $SiN_x$ and ~96% for the cell with 2000 Å thick $SiN_x$. Note that there is ~3% discrepancy between simulated and measured $R_b$ due to the Al-BSF lines on the back which are not as reflective. The 8% Al-BSF only has ~65% BSR value which lowers the effective BSR on the back to 96% (8% ×65% + 92%×99% ≈ 96%). According to our roadmap (Figure 4.5), 96% BSR value with 2000Å thick $SiN_x$ on the rear side satisfies the requirement for ~21% PERC cell.

**Table 8.6 Best and average results of PERC cells (7 wafers per each group) with two different rear $SiN_x$ thickness.**

| Rear $SiN_x$ thickness (Å) | $R_b$ (%) | | $V_{oc}$ (mV) | $J_{sc}$ (mA/cm$^2$) | FF (%) | η (%) |
|---|---|---|---|---|---|---|
| 1600 | 95% | average | 665 | 38.5 | 79.4 | 20.3 |
| | | best | 667 | 38.6 | 79.6 | 20.5 |
| 2000 | 96% | average | 666 | 38.7 | 79.4 | 20.5 |
| | | best | 667 | 38.8 | 79.6 | 20.6 |

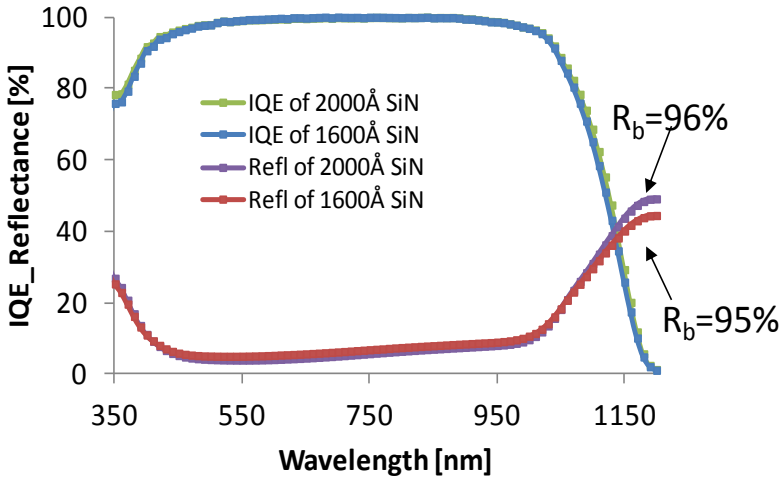



**Figure 8.22 IQE and Reflectance curves of PERC cells with 1600 Å and 2000 Å thick $SiN_x$ layers on the rear side as back surface reflector.**

## 8.4 Development of Manufacturable Line Contact Geometry on the Back Side of the PERC Cell

### 8.4.1 Contact Opening through the Dielectric Stack Using UV Laser

This section focuses on developing local line contacts on the back side instead of point contacts (developed in the Chapter 6) to enhance rear contact quality, cell manufacturability and throughput using our UV laser tool. As discussed in the Chapter 6, the optimal design of the rear contact is a function of the contact geometry (spacing and width) contact resistance and recombination velocity. In the GEN-I PERC cell, 130µm×130 µm vias were ablated through the rear dielectric stack ($SiO_2/SiN_x$) using a Coherent UV laser (355 nm) with a nanosecond pulse-width and a Gaussian beam profile. Figure 8.23 shows the dependence of the dielectric opening width on the laser energy using one laser pulse. Higher laser energy creates a wider via opening. One laser pulse with 200 µJ creates ~75 µm wide contact while four laser pulses with ~20 µm overlap produce~130 µm wide contact. It was challenging to make uniform local BSF through75 µm wide vias; therefore, four 200µJ laser pulses with repetition rate of 60 kHz were used to open the 130 µm wide square contacts with 500 µm spacing in Phase-I for the development of GEN-I cells.

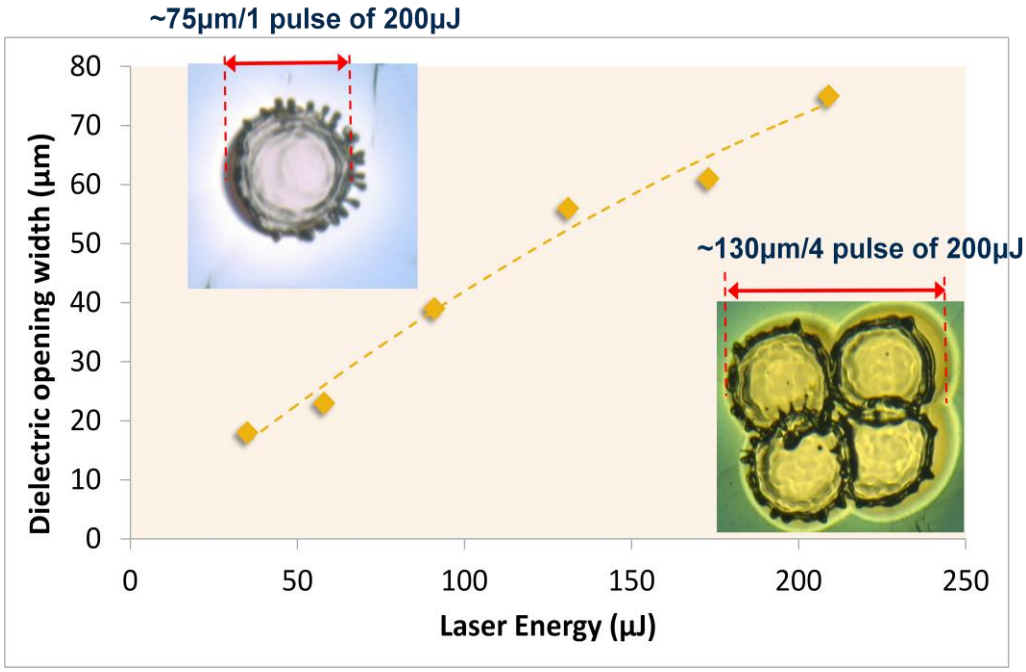



**Figure 8.23 Dielectric opening widths versus one laser pulse energy and optical microscope image of typical via defined using UV laser 1 pulse (up-left) and 4 pulses (bottom-right).**

The above point contact geometry (point) is time consuming because it took about four minutes to perform laser ablation on a commercial size 239 $cm^2$ Cz Si wafer. In addition, it was found that the BSF was non-uniform and got very thin (~2-3 um) near the edges of the vias (Figure 8.24). The thin BSF around the contact can lead to parasitic shunts in the presence of inversion layer. For these reasons, line contacts using a single pulse with optimal contact spacing was used to increase the throughput, and uniformity of local BSF.

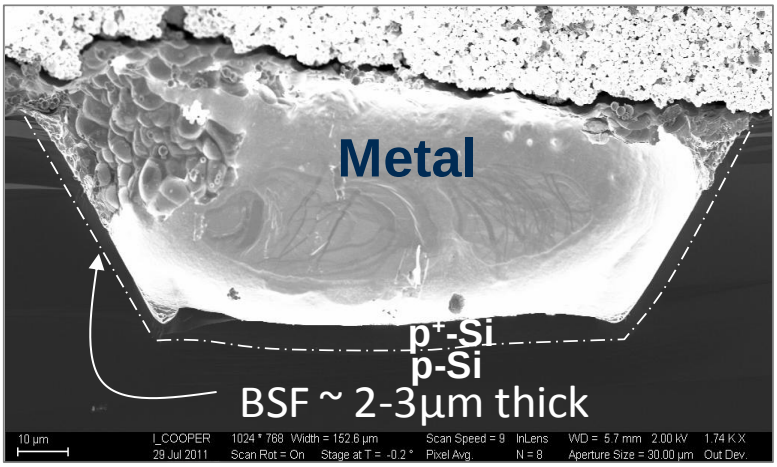



**Figure 8.24 SEM image of point contact and BSF obtained using ablation with four pulses of UV laser.**

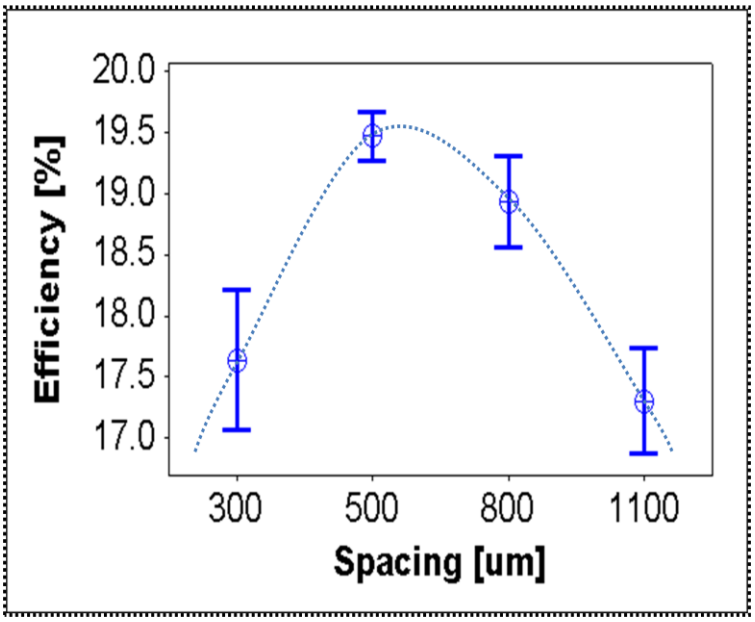



**Figure 8.25 Efficiency data for PERC cells with 130 µm point contact width and various contact spacing (reproduction of Figure 6.11).**

### 8.4.2 Design and Optimization of Line Contact Geometry for High Efficiency PERC Cell

In order to optimize the rear line contact geometry, a 2-D device model of Meemongkolkiat [13] was used to establish the optimum spacing and opening for the lines. Figure 8.27 shows a 3-D cell structure he used to simulate solar cell performance using Sentaurus device modeling software. He calculated cell efficiency as a function of contact spacing (300 to 2000 µm) and SRV (300 to $10^6$ cm/s) at the p-p+ interface for 75 and 150 µm wide lines. Calculated an optimal spacing was ~500 µm for the 75 µm wide line contacts and ~1000 µm for the 150 µm wide line contacts for lower SRV values. Meemongkolkiat's simulations also showed that the use of line contacts provides a much wider process window for fabricatiing high efficiency devices.

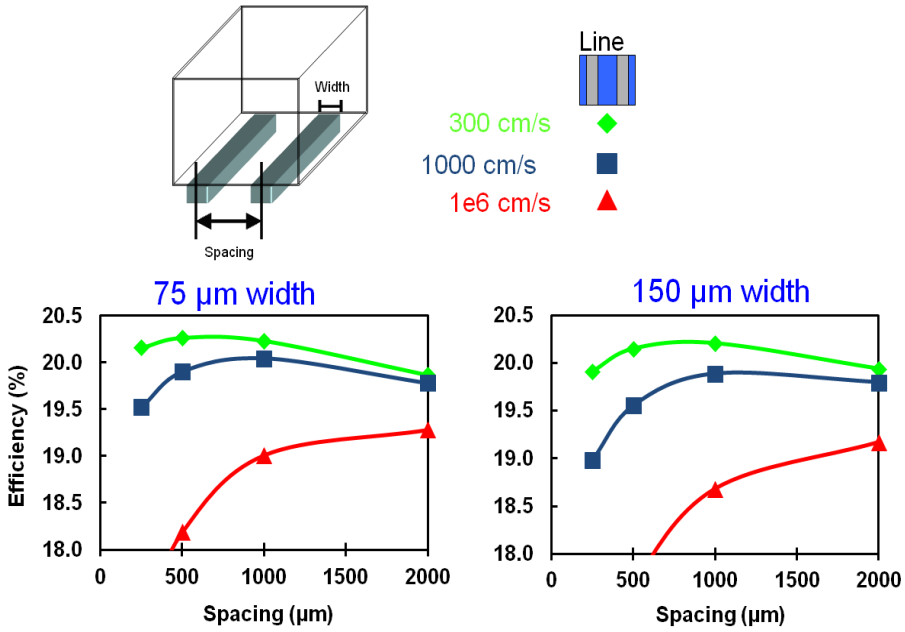



**Figure 8.26 2-D modeling results for PERC cells with line rear contact geometries [13].**

In this section attempts were made to validate Meemongkolkiat's modeling by implementing line contacts on the rear side of the PERC cells. As mentioned earlier, one of the goals of this study is to increase UV laser throughput by implementing simpler patterning with a single pulse. In our laser setup, 75 µm wide line opening required only single pulse and two pulses for 150 µm wide opening. Figure 8.27 shows an optical microscope image of the 75 µm wide line contact defined using one ~200 µJ UV laser pulse with the repetition rate of 60 kHz.

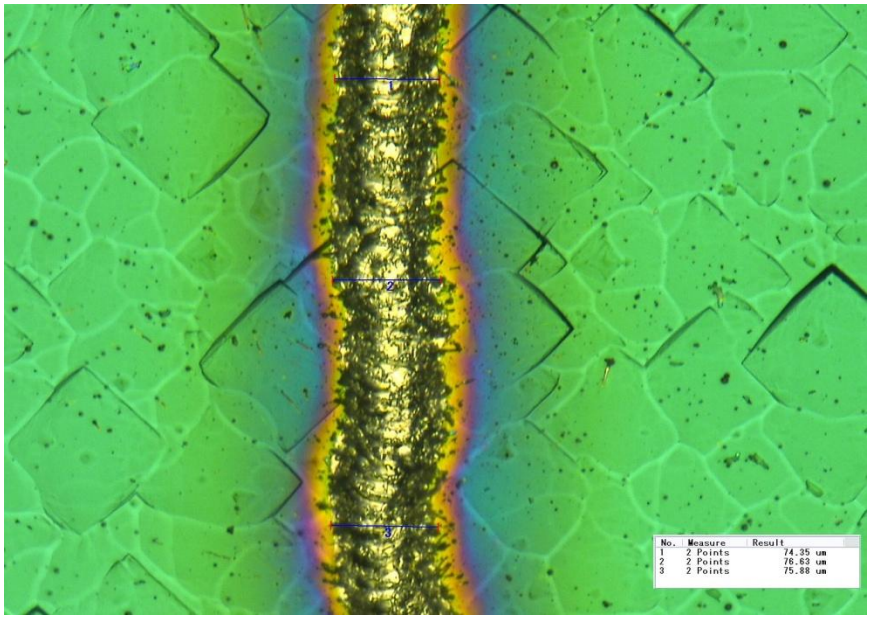



**Figure 8.27 Optical microscope image of 75 µm line contact opening defined by single UV laser pulse.**

Figure 8.28 shows the SEM cross section of a line contact after cleaving the sample. The BSF around the metal contact is highlighted by dashed line in Figure 8.28. The uniformity and thickness of the BSF for the line contact were found to be superior than the point contact which had regions of only 2-3 µm BSF (Figure 8.24). Line contacts showed ~5-6 µm deep BSF which is adequate for good BSRV at the p-p+ interface. The

formation of a thick and continuous BSF is important for high efficiency PERC cells, and it also helps in avoiding the parasitic shunting in the device. Thus the line contact geometry not only increases throughput but also provides more uniform BSF compared to the point contacts in the GEN-I PERC cell. This is also a more commercially viable option for fabricating high efficiency PERC cells.

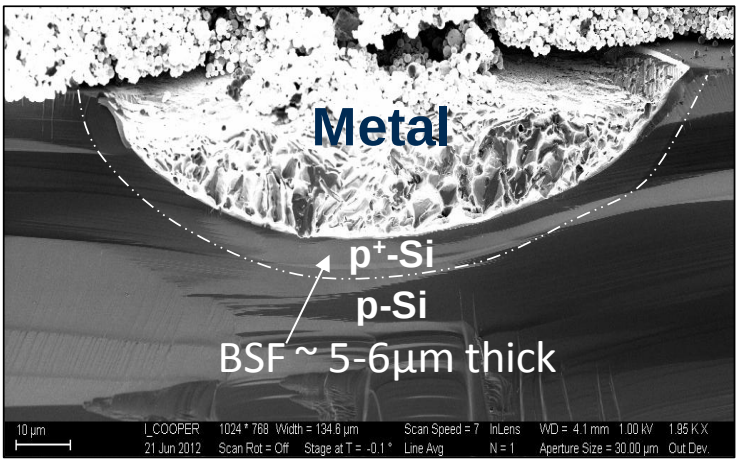



**Figure 8.28 SEM image of line contact and BSF obtained using ablation with one pulse UV laser. The BSF around the contact metal was illustrated by dashed line**

To validate the 2-D modeling results of Meemongkolkiat [13], PERC cells with 75 µm wide line contacts were fabricated with different line spacing in the range of 500 to 1400 µm (Table 8.7). Best cell efficiency of 20.6% was achieved with 1000 µm spacing for 75 µm wide lines. The trend in $V_{oc}$, $J_{sc}$, FF, $R_s$ and efficiency for different line spacing are shown in Figure 8.29. Increasing the line spacing increases the resistive loss but decreases the contact recombination, which in turn increases the series resistance and $V_{oc}$ but lowers the fill factor resulting in an optimal spacing of 1000 µm for the 75 µm wide lines.

**Table 8.7 I-V parameters for the PERC cells (five wafers per each group) with different line contact spacing on the rear side.**

| Spacing (μm) | | $V_{oc}$ (mV) | $J_{sc}$ (mA/cm$^2$) | FF (%) | η (%) | $R_s$ (Ω.cm$^2$) |
|---|---|---|---|---|---|---|
| 500 | average | 656 | 38.7 | 78.7 | 20.0 | 0.70 |
| | best | 659 | 38.8 | 78.9 | 20.2 | 0.81 |
| 800 | average | 662 | 38.9 | 78.3 | 20.1 | 0.76 |
| | best | 663 | 39.1 | 78.4 | 20.3 | 0.80 |
| 1000 | average | 664 | 39.1 | 78.7 | 20.4 | 0.76 |
| | best | 664 | 39.1 | 79.2 | 20.6 | 0.66 |
| 1200 | average | 663 | 39.0 | 77.9 | 20.2 | 0.81 |
| | best | 668 | 38.9 | 78.6 | 20.4 | 0.91 |
| 1400 | average | 663 | 39.0 | 77.4 | 20.0 | 0.86 |
| | best | 669 | 39.2 | 78.3 | 20.5 | 0.91 |

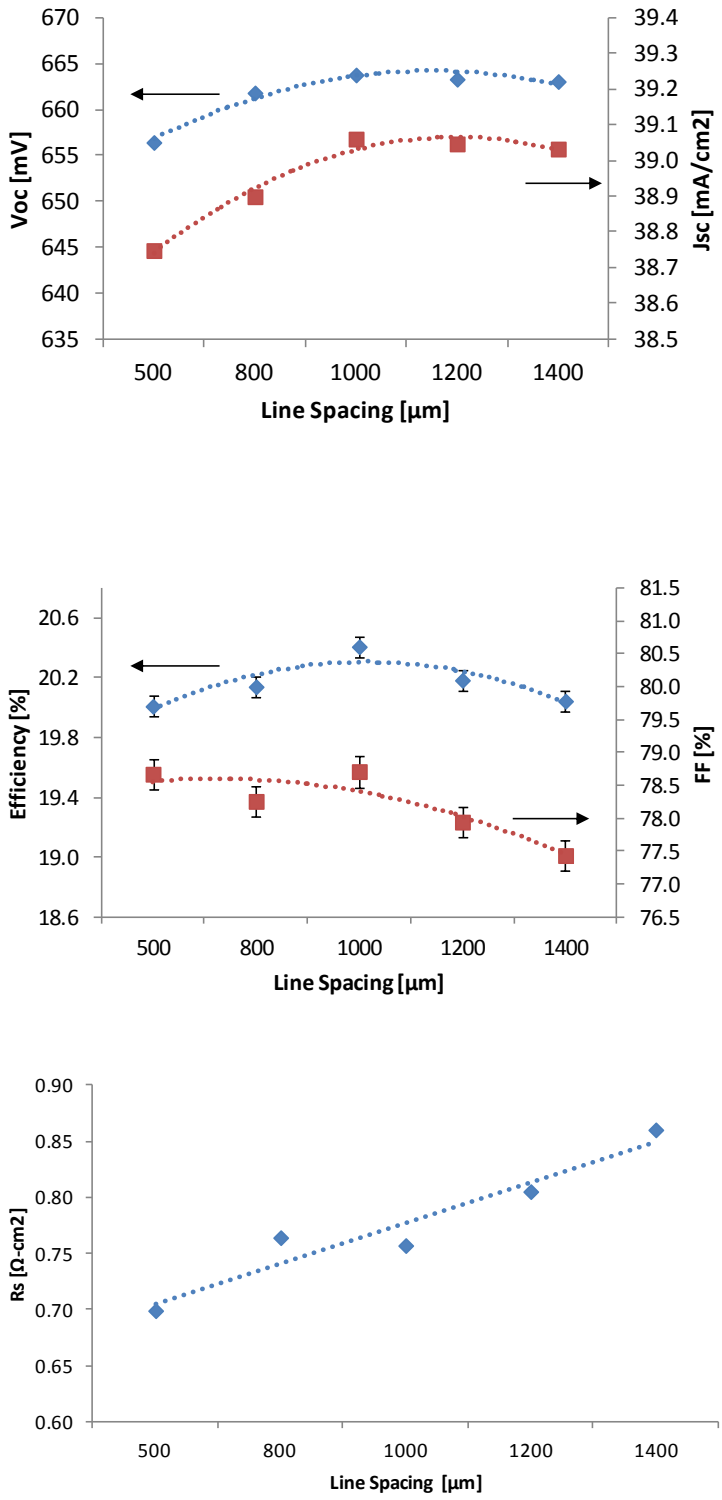
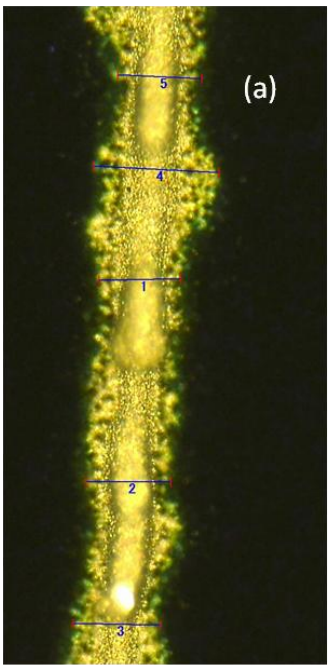



**Figure 8.29 $V_{oc}$, $J_{sc}$, FF, Efficiency and $R_s$ trends for the PERC cells with different line spacing on the rear side.**

## 8.5 Development of Fine Line Screen Printing Technology to Reduce Shading Loss in High Efficiency PERC Cell

In Chapter 7, we demonstrated that fine line direct print technology can reduce the shading to 5.5% and give appreciable improvement in cell efficiency. However, the nScrypt tool is not commercially available for mass production of solar cells. Therefore, we decided to improve screen-printing technology with the help of emerging Ag pastes and improved screen material and design. We reduced the screen opening from 55 µm to 40 µm and applied newer pastes from DuPont and Heraeus. This shrunk the line width from ~80 µm to ~60 µm as shown in Figure 8.30 (a). However, considerable non-uniformity was observed in the line height (average of ~15 µm), as shown in the 3-D microscope image below (Figure 8.30 (b)).




| No. | Measure | Result |
|---|---|---|
| 2 | 2 Points | 58.33 um |
| 3 | 2 Points | 60.25 um |
| 4 | 2 Points | 86.66 um |
| 5 | 2 Points | 58.01 um |

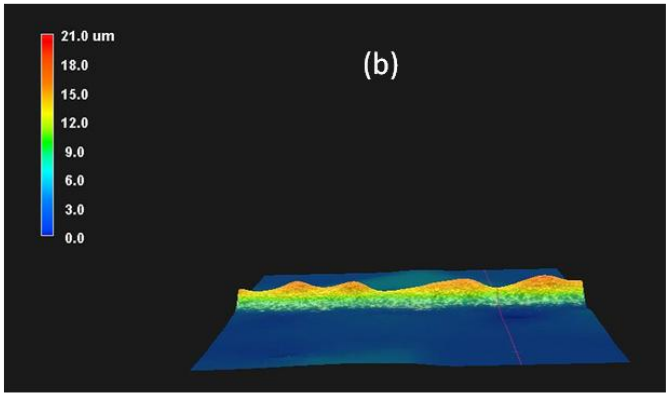



**Figure 8.30 Optical microscope image of a narrow screen printed finger.**

To understand the impact of the non-uniform printing on series resistance, a detailed series resistance analysis was performed on a PERC cell to determine the six components of $R_s$ [112]: $R_s$(busbar), $R_s$ (gridline), $R_s$(front contact), $R_s$(emitter sheet), $R_s$(substrate), and $R_s$(back contact). The detailed expressions for calculating each series resistance component can be found in [120].

Figure 8.31 shows each component of $R_s$ in the PERC cell made with narrow screen opening in this study. Clearly, the gridline resistance dominates the series resistance and accounts for ~60% of the total $R_s$ value. This is attributed to the non-uniform height of screen-printed lines.

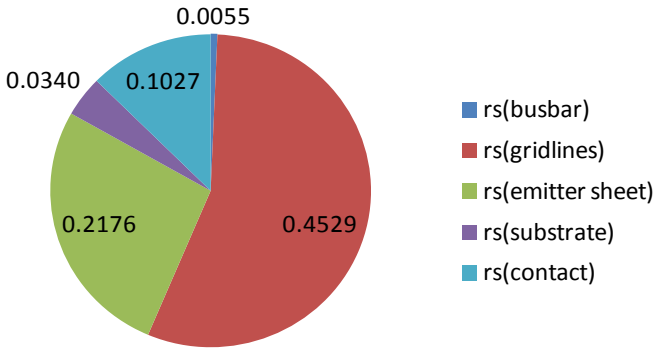



**Figure 8.31 Series resistant components for a PERC cell with screen-printed Ag gridlines (~60 µm wide).**

According to the roadmap (in Chapter 4), a FF of > 79.5% is required to achieve 21% efficiency. In addition, the total $R_s$ needs to be ~0.6 Ω-cm$^2$ while maintaining < 6% shading. Our gridline model analysis shows that increasing the line height from 15 µm to ~25 µm while maintain the line width of 60 µm, can lower the gridline resistance from

0.45 Ω-cm$^2$ to 0.26 Ω-cm$^2$ and should result in total Rs ~0.6 Ω-cm$^2$ (discussed in more detail in Chapter 10).

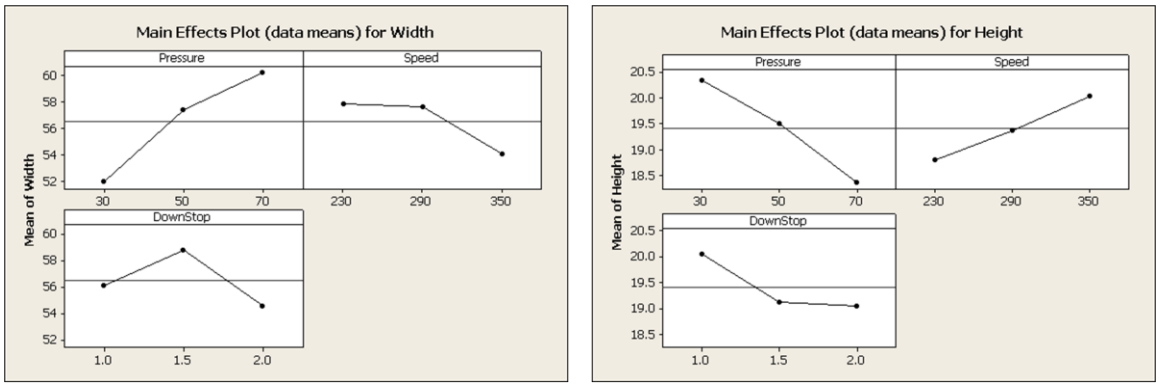
To achieve the above requirements, a three-level full factorial experiment was designed and conducted to study the effect of three key screen printing parameters, namely pressure, speed, and down stop on the gridline width and height. The experiment was carried out according to the design matrix shown in the Table 8.8. The printing pressure was varied between 30 to 70 NT; the printing speed was ranged from 230 to 350 mm/s; and down stop was varied between 1 to 2 mm. The down stop is the depth to which the squeeze presses down the screen during printing. The line width and line height were measured by Keyence microscope on the three sampling points over a wafer after firing the Ag gridlines. MINITAB statistical software was used to analyze the line width and line height data. The detail of statistical calculations and analysis can be found in [106].

**Table 8.8 Factors and levels for fine line screen printing experiment.**

| Factor | Level | Values |
|---|---|---|
| Pressure (NT) | 3 | 30, 50, 70 |
| Speed (mm/s) | 3 | 230, 290, 350 |
| Down Stop (mm) | 3 | 1.0, 1.5, 2.0 |

Figure 8.32 shows the main effect plot for each process parameter. Figure 8.32 (a) shows their effect on line width and Figure 8.32 (b) shows their effect on line height. The horizontal axis of the plot represents three levels or values for each process parameter

(Table 8.8) while the vertical axis represents the average line with or line height. The data in Figure 8.32 show that as pressure or speed decreases, the line width decreases and line height increases. This is good for aspect ratio and front side metal coverage. However, as down stop increases, the line width increases but the line height increases. Based on this analysis, we conclude that the optimal printing parameters for fine line screen printing should include low pressure (30 NT), low speed (230 mm/s), and low down stop (1 mm). This was validated by applying these optimized parameters simultaneously which indeed resulted in very narrow (~57 µm) and tall (~21 µm) gridlines (Figure 8.33). Next step was to integrate all the technology enhancements developed in this chapter into a process sequence to fabricate the GEN-II PERC cells.




(a) (b)

**Figure 8.32 (a) Main effect plot for line width. (b) Main effect plot for line height.**

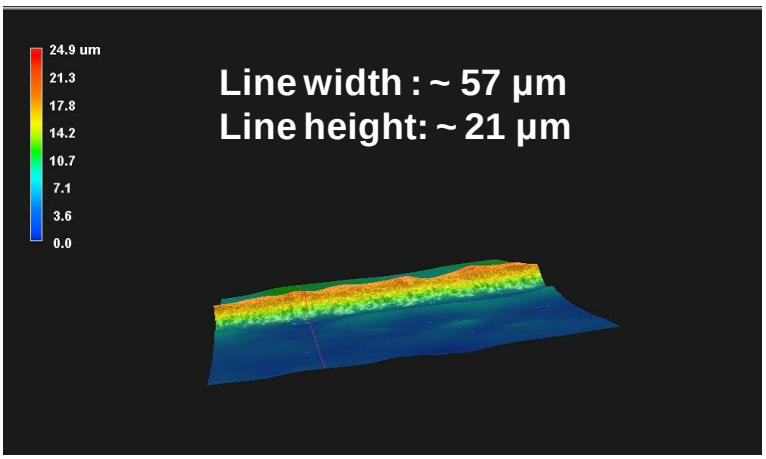



**Figure 8.33 3D microscope image of narrow and high screen printed gridlines using optimal process parameters of pressure (30 NT), low speed (230 mm/s), and low down stop (1 mm).**

## 8.6 Successful Fabrication and Characterization of ~21% PERC Cells

In the previous five sections, we developed and demonstrated five technology enhancements for raising the PERC cell efficiencies. These enhancements involved low-cost homogeneous emitter with reduced emitter recombination ($J_{oe}$~130 cm/cm$^2$), optimized back oxide thickness with low surface recombination (BSRV~100cm/s), optimized implant dose ($2.8\times10^{15}$ cm$^{-2}$) to reduce low resistive loss (FF~79.5%), optimized back surface reflector with thicker $SiN_x$ to increase BSR (> 95%), high quality and high throughput rear line contacts, and improved screen-printed contacts with narrow grid lines (~60 µm wide). All the above developments were integrated into the process sequence shown in Figure 8.34 to achieve ~21% efficient PERC cells.

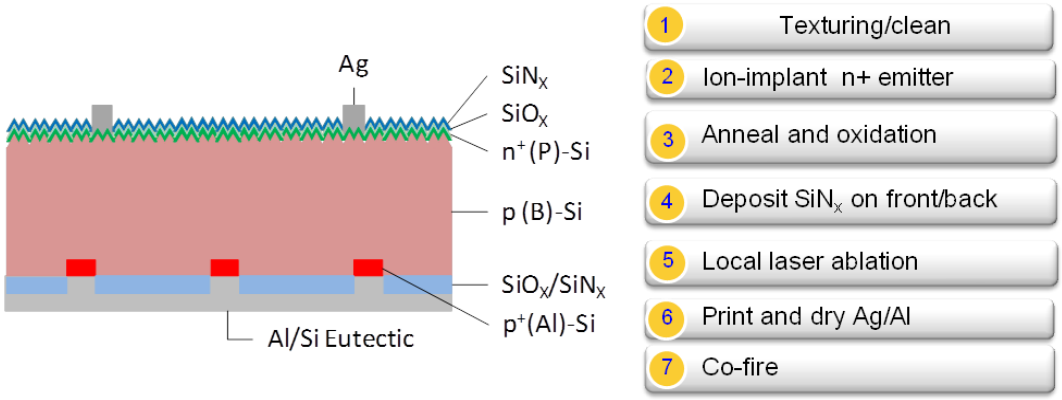



**Figure 8.34 Cell structure and process sequence for PERC cell**

Table 8.9 shows that the best cell efficiency of 20.8% was achieved for the GEN-II PERC cell in this study. Combined effect of all the optimized parameters (Figure 8.35), namely ~90 Ω/sq homogeneous emitter, 80 Å oxide thickness, 75 µm rear line contacts with 1 mm spacing, 2000Å thick $SiN_x$ on the rear side for BSR, and 60 µm wide narrow gridlines, resulted in 11 mV improvement in $V_{oc}$, 0.7 mA/cm$^2$ improvement in $J_{sc}$ , 0.3 % increase in FF compared to the GEN-I screen-printed PERC cell ($V_{oc}$ of 656 mV, $J_{sc}$ of 38.3 mA/cm$^2$, FF of 79.2%). Figure 8.36 shows the evolution of implied open-circuit voltage as a function of process steps. The 20.8% efficient PERC cell had $V_{oc}$ of 667 mV, $J_{sc}$ of 39.1 mA/cm$^2$, and FF of 0.798. Table 8.9 also shows that the average of 15 cells was 20.6%. This demonstrates that the fundamental understanding and the technology enhancements in this research were successful in bringing the large-area screen-printed PERC cell efficiency close to 21%.

**Table 8.9 I-V data of a 20.8% efficient PERC cell on 239cm$^2$ p-type Cz Si wafer, along with the PC1D simulated I-V data. Also shown is the average I-V data for the 15 cells.**

| | | $V_{oc}$ (mV) | $J_{sc}$ (mA/cm$^2$) | FF (%) | η (%) |
|---|---|---|---|---|---|
| Best cell | Measured | 667 | 39.1 | 79.8 | 20.8 |
| | PC1D | 665 | 39.2 | 79.8 | 20.8 |
| Ave. of 15 cells | Measured | 666 | 39.0 | 79.2 | 20.6 |

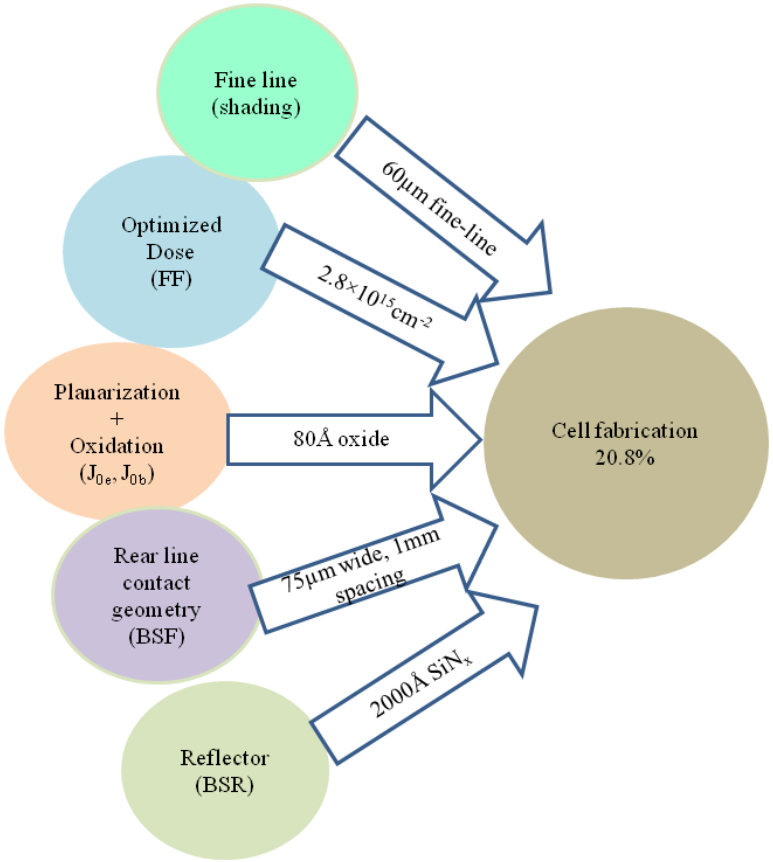



**Figure 8.35 All the optimized parameters, namely ~90 Ω/sq homogeneous emitter, 80 Å oxide thickness, 75 μm rear line contacts with 1 mm spacing, 2000Å thick $SiN_x$ as a BSR, and 60 μm wide narrow gridlines, to achieve the 20.8% efficient PERC cell.**

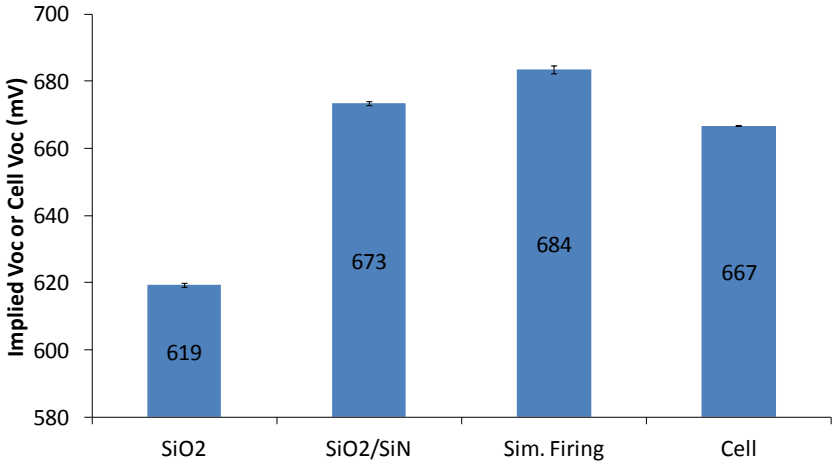



**Figure 8.36 Evolution of implied Voc as a function of process steps.**

To gain deeper insight into efficiency enhancements in the GEN-II PERC cell, the 20.8% efficient cell was characterized and modeled in detail using the PC1D device modeling program. Table 8.10 shows the set of measured input parameters used into the PC1D model that matched the measured and modeled I-V and IQE of the 20.8% cell. The extracted parameters for the 20.8% cell are also listed in the same table. Table 8.10 also lists the parameters required to achieve the 21% cell that were established in Chapter 4 by PC1D modeling. The detailed analysis revealed that the GEN-II PERC cell has front surface recombination velocity (FSRV) of 10,000 cm/s and the back surface recombination velocity (BSRV) of 100 cm/s, which were extracted by matching the measured IQE and the simulated IQE in the short wavelength (< 600 nm) and long wavelength (900-1,200 nm) range (Figure 8.37). The back surface reflectance (BSR) of 96% was extracted by matching the measured escape reflectance in the long wavelength (> 1000 nm). The above values are very close to the target values for FSRV (8,000 cm/s), BSRV (100 cm/s) and BSR (96%) to achieve 21% efficient cell. The PC1D modeling predicted a cell efficiency of 20.8% with $V_{oc}$ of 665 mV, $J_{sc}$ of 39.2 mA/cm$^2$, and FF of 79.8% which are in good agreement with the measured I-V values (Table 8.9). Thus the

cell results validate the modeling and confirm the efficiency enhancements from multiple technology developments.

**Table 8.10 PC1D modeling of the 20.8% GEN-II PERC cell and target parameters for 21% cell.**

| Cell Parameters | 20.8% GEN-II PERC cell | 21.1% Target |
|---|---|---|
| Wafer thickness (μm) | 180 | 180 |
| Base Resistivity (Ω-cm) | 2.0 | 2.0 |
| RSERIES (Ω-cm2) | 0.6 | 0.6 |
| $R_{SHUNT}$ (Ω-cm$^2$) | 41667 | 41667 |
| $N_2$ | 2.2 | 2.2 |
| $J_{02}$ (nA/cm$^2$) | 20 | 20 |
| Emitter sheet resistance(Ω/sq) | 90 | 150 |
| Junction Depth (μm) | 0.35 | 0.30 |
| Surface concentration (cm$^{-3}$) | $2.0\times10^{20}$ | $7.4\times10^{19}$ |
| Texture angle (degrees) | 54.74 | 54.74 |
| Texture depth (μm) | 3.535 | 3.535 |
| Rear surface charge (cm$^{-2}$) | $2.2\times10^{11}$ | $2.2\times10^{11}$ |
| $t_{bulk}$ (μs) | 500 | 500 |
| BSRV (cm/s)/ $J_{ob}$ (fA/cm$^2$) | 100 /97 | 100 /97 |
| FSRV (cm/s)/ $J_{oe}$ (fA/cm$^2$) | 10000 /179 | 8000 /133 |
| $R_{back}$ (%) | 96 | 96 |
| Grid shading (%) | 6.3 | 5.5 |
| Modeled $V_{OC}$ (mV) | 665 | 670 |
| Modeled $J_{SC}$ (mA/cm$^2$) | 39.2 | 39.5 |
| Modeled FF (%) | 79.8 | 79.7 |
| Modeled Efficiency (%) | 20.8 | 21.1 |

(*Measured $V_{oc}$ = 661mV, $J_{sc}$ = 39.1 mA/cm$^2$, FF = 79.8%, η = 20.8%)

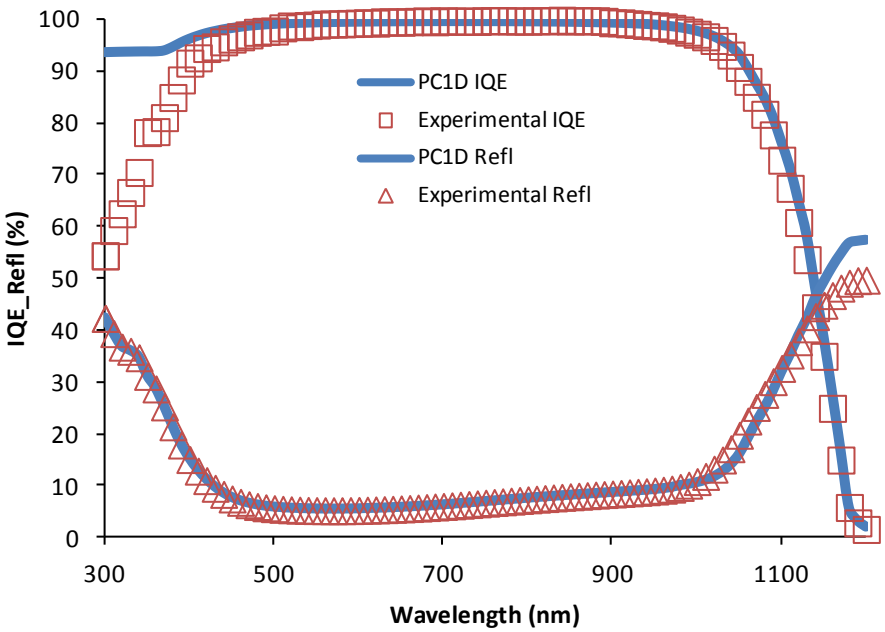



**Figure 8.37 PC1D fits to the measured IQE and reflectance of a 20.8% efficient PERC cell.**

## 8.7 A Study of Light Induced Degradation in PERC Cells

It is well known that p-type boron-doped Cz silicon cells suffer from light-induced degradation (LID) due to the formation of boron-oxygen (B-O) complexes in the bulk [121]. These complexes form point defects which act as recombination sites in the wafer and hence degrade carrier lifetime. Even though the bulk lifetime degradation may be same under identical light soaking conditions but its impact on cell efficiency may not be same for different cell structures. It has been reported that LID degrades cell efficiency by 0.2-0.5% absolute in current baseline cell with full aluminum back surface field (Al-BSF) cells. However, the impact of LID increases on advanced cell devices like PERC because bulk lifetime or diffusion length degradation tends to decouple the back

surface passivation, which is instrumental in enhancing efficiency of PERC devices [122].

Figure 8.38 shows the comparison of LID in PERC and the baseline Al-BSF cells fabricated in this study. The PERC cell lost ~0.8% absolute cell efficiency, while the efficiency of baseline cell dropped by only ~0.5% after 72 hours of illumination. This agrees well with the modeling done by Das et al. [122] which predicted greater loss in PERC cells. To achieve higher stabilized efficiency on p-type PERC cells one needs to either reduce oxygen content of the wafer or replace B dopant by another Group III element, such as Ga or In. Therefore, in the next chapter, we will evaluate for the first time the efficiency potential and LID in In-doped PERC cells.

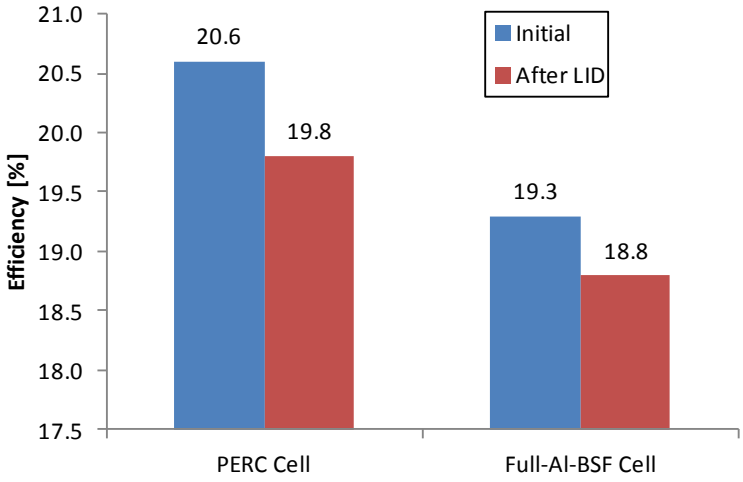



**Figure 8.38 Comparison of LID effect for the PERC cell and baseline Al-BSF cell.**

## 8.8 Summary

By developing and integrating multiple efficiency enhancement features, namely low-cost high sheet resistance homogeneous emitter, optimized surface passivation, optimized rear reflector, back line contacts, and improved screen-printing with narrow grid lines, 20.8% efficient screen-printed GEN-II PERC cells were achieved on

commercial grade 239 $cm^2$ p-type Cz Si wafers. These enhancements (Figure 8.39) resulted in a 0.8% (absolute) efficiency enhancement over the GEN-I PERC cell (20%) and a 2.5% (absolute) efficiency enhancement over the baseline full Al-BSF cell (18.3%). Table 8.11 summarizes all the key technology developments and their corresponding efficiency enhancements that raised the baseline cell efficiency from 18.3% to 20.8% on commercial grade 239 $cm^2$ Cz Si wafers. Detailed PC1D modeling and analysis showed that the GEN-II PERC had a FSRV of 10,000 cm/s, BSRV of 100 cm/s, BSR of 96%, and grid shading of 6.3%. These values are very close to the parameters established by PC1D device modeling to achieve ~21% cell. Next chapter will provide guidelines for future work that can raise the PERC cell efficiency to 22%.

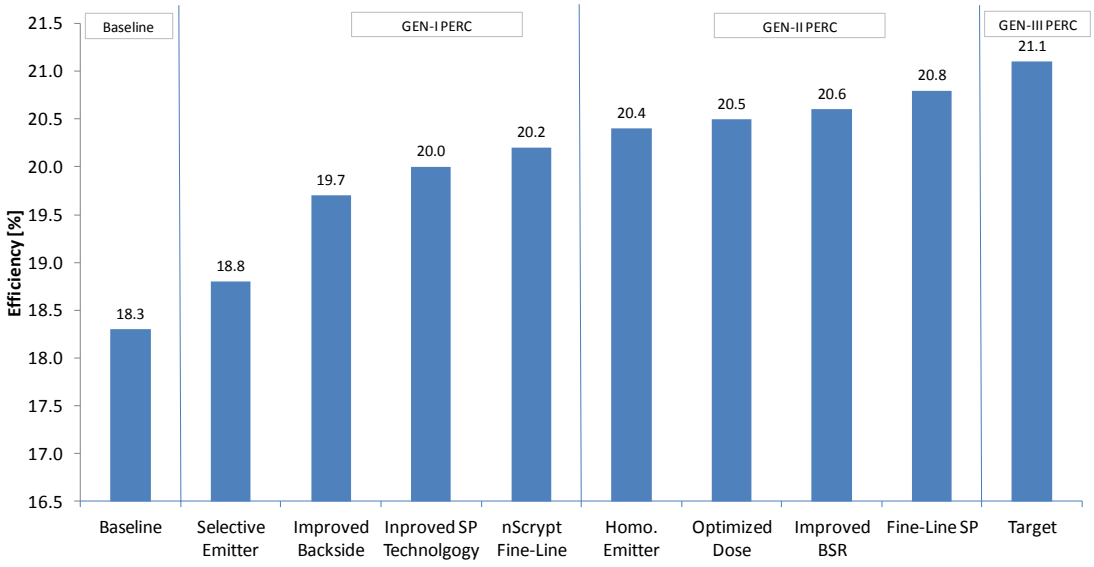



**Figure 8.39 Various technology development and innovations that contributed to efficiency enhancement from 18.3% to 20.8% on commercial grade 239 $cm^2$ Cz Si wafers.**

**Table 8.11 Efficiency enhancement from each key technology development that contributed to increase in cell efficiency from 18.3% to 20.8%.**

| Cell type | Key Development | Efficiency enhancement (%) | Efficiency (%) |
|---|---|---|---|
| Baseline | Commercial grade Cz Si full Al-BSF cell | 0.0 | 18.3 |
| GEN-I | Selective emitter | +0.5 | 18.8 |
| | Improved rear passivation, BSR, LBSF | +0.9 | 19.7 |
| | Improved screen printing technology | +0.3 | 20.0 |
| | Fine-line direct printing technology | +0.2 | 20.2 |
| GEN-II | High sheet resistance homogeneous emitter | +0.4 | 20.4 |
| | Optimized implant dose | +0.1 | 20.6 |
| | Improved BSR | +0.1 | 20.6 |
| | Improved screen printing technology | +0.2 | 20.8 |
| | Line contact geometry | throughput | 4 times ↑ |

# CHAPTER 9

# USE OF INDIUM DOPING TO MITIGATE LIGHT INDUCED DEGRADATION IN HIGH EFFICIENCY P-TYPE PERC SILICON SOLAR CELLS

In Chapter 8, we showed that the PERC cells exhibit greater light induced efficiency degradation (LID) compared to the baseline cells in spite of the same lifetime degradation caused by B-O complex formation. This negates some of the efficiency advantage of the PERC cells. This chapter discusses a novel and promising approach to make nearly LID free PERC cells by using indium-doped Cz Si substrates.

## 9.1 Review of Light Induced Degradation

Solar cells based on p-type boron-doped Cz silicon suffer light-induced degradation (LID) due to the formation of boron-oxygen (B-O) complexes in the bulk [121, 123-125]. These complexes degrade carrier lifetime and cell efficiency by 0.2-0.5% absolute in baseline full aluminum back surface field (Al-BSF) cells. However, PERC cells are more vulnerable to LID because part of its efficiency enhancement comes from excellent back surface passivation. The LID degrades bulk lifetime or diffusion length of the PERC cell with tends to decouple the back surface passivation. Therefore, one needs to reduce either oxygen concentration or replace B dopant by another Group III acceptor, such as Ga or In to achieve stabilized high efficiency PERC cells. Considerable research has been done on reduction of oxygen and incorporation of Ga dopant [126-129]. However, very little is known about the performance of In-doped Si cells. This chapter

reports for the first time on the stabilized performance of large-area, In-doped baseline as well as PERC cells to demonstrate their LID superiority over the B-doped PERC cells.

## 9.2 Application of PERC Technology to Indium-Doped CZ Si Materials

In this study, ~3.1 Ω-cm indium-doped monocrystalline wafers (Set A) were produced at SunEdison using a Continuous Cz method. For comparison, two commercial grade boron-doped ongots were included in this study. First B-doped ingot (Set B) had high lifetime of ~600 μs and high oxygen (21 ppma) concentration and the second B-doped ingot (Set C) had ~14 ppma oxygen and a bulk lifetime of ~300 μs. The resistivity of both B-doped ingots were in the range of 1.5 - 2.7 Ω-cm. All three ingots produced had 239 $cm^2$ pseudo square wafers. Standard baseline cells with full Al-BSF as well as advanced PERC cells with dielectric back passivation and local BSF (Figure 9.1) were fabricated using the process sequence described in previous chapters. These cells were characterized and analyzed before and after 0.7 sun 72-hour of illumination to study the LID behavior.

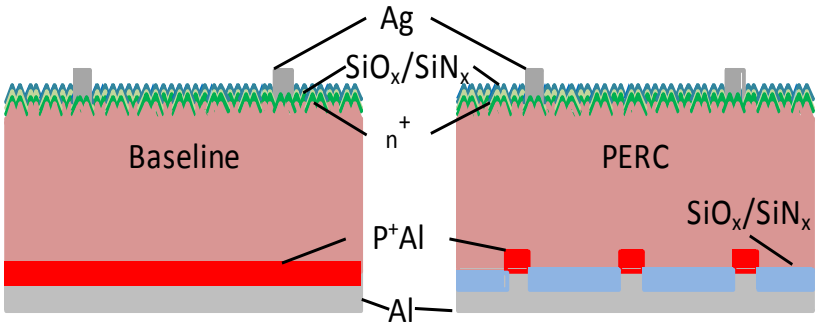



**Figure 9.1 Structure of baseline (left) and PERC (right) cells.**

The fabrication process of the PERC cell involved saw damage removal in a heated KOH solution followed by alkaline texturing of both sides of the silicon wafers. Then, one side was planarized using an alkaline solution. Ion implantation energy, dose and anneal conditions were selected to achieve a homogeneous emitter with ~90 Ω/sq. sheet resistance. An in-situ, thin oxide was grown on both surfaces during the implant anneal. A PECVD $SiN_x$ film was deposited on the front and rear sides to cap the oxide. Then a UV laser (355 nm wavelength with nanosecond pulse width) was used to open lines through the rear dielectric stack. Finally, Ag grid was screen printed on the front and full Al on the rear followed by co-firing of the front and back contacts in a belt furnace.

The light IV data was obtained on a tester calibrated using Fraunhofer traceable cells. Following the initial IV characterization, few cells from each set were placed under a halogen light bank for 72 hours at ~0.7 suns at 45˚C for LID evaluation. A Light Beam Induced Current (LBIC) scan with a 980 nm laser was performed to characterize the recombination activity. The bulk lifetime was measured on blanket wafers using the QSS-PC method at an injection level of $5\times10^{14}$ $cm^{-3}$. FTIR measurements were performed to assess the $O_i$ concentration in the samples.

## 9.3 Comparison of Efficiency and LID in Indium- and Boron-Doped Cz Si Cells

### 9.3.1 Material Characteristics of In- and B-doped Wafers

Table 9.1 shows resistivity, bulk lifetime and oxygen concentration of the In- and B-doped wafers used in this study. The measured interstitial oxygen concentration was about 12 ppma in In-doped wafers, whereas B-doped Sets B and C measured about 21 ppma and 14 ppma, respectively. Effective lifetimes were measured to be 172 μs, 600 μs and 320 μs on wafers from In and two B-doped wafers (Set A, B, and C). Note that the B-doped wafers in Set B have the highest oxygen concentration as well as the highest lifetime, while the In-doped wafers in Set A have the lowest lifetime and the lowest oxygen concentration (Table 9.1).

**Table 9.1 Resistivity, interstitial oxygen concentration and bulk lifetime in In-doped and B-doped wafers.**

| Set | Dopant Type | Resistivity (Ω-cm) | ($O_i$) ppma | Lifetime (μs) @ 5E14cm$^{-3}$ |
|---|---|---|---|---|
| A | Indium | 3.1 | 12.8 | 172 |
| B | Boron | 1.5 | 21.6 | 600 |
| C | Boron | 2.7 | 14.8 | 320 |

### 9.3.2 Efficiency Comparison of Baseline In- and B-Doped Solar Cells before and After LID

Table 9.2 shows the baseline cell efficiency on In- and the two B-doped wafers before and after the LID. It is interesting to note all three cells gave 19.1~19.3%

efficiency. However, after the light-induced degradation, cell efficiency of both B-doped dropped significantly (~0.5%). In contrast, In-doped cells showed no appreciable loss in cell efficiency ($\leq$ 0.1%) due to LID and resulted in ~0.4% higher in absolute efficiency after light exposure or stabilization.

**Table 9.2 Cell efficiency of baseline cells and In- and B-doped wafers before and after light induced degradation.**

| Ingot | Dopant Type | | $V_{oc}$ (mV) | $J_{sc}$ (mA/cm$^2$) | FF (%) | $\eta$ (%) |
|---|---|---|---|---|---|---|
| A | Indium | Initial | 636 | 37.6 | 79.8 | 19.1 |
| | | LID | 635 | 37.5 | 79.7 | 19.0 |
| B | Boron | Initial | 642 | 37.6 | 79.7 | 19.3 |
| | | LID | 636 | 37.2 | 78.9 | 18.7 |
| C | Boron | Initial | 641 | 37.4 | 79 | 18.9 |
| | | LID | 634 | 36.9 | 78.4 | 18.4 |

### 9.3.3 Efficiency Comparison of In- and B-Doped Advanced PERC Solar Cells Before and After LID

Table 9.3 shows average and best cell efficiency of PERC cells from In-doped wafers (Set A), and the two B-doped wafers (Sets B and C). Unlike the full Al-BSF cells, where initial cell efficiency for all three sets was similar, a difference exists in the initial efficiencies of PERC cells. Because within PERC cells, where the passivated rear surface alleviates a significant portion of the surface recombination, the sensitivity to bulk and front surface recombination mechanisms becomes greater. The indium-doped substrates exhibited an initial PERC cell efficiency of 20.0% compared with 20.5% and 20.2% from

boron sets B and C. This is the first time an efficiency of 20% has been achieved and reported on large-area In-doped solar cells. Using indium as a replacement acceptor for boron still requires optimization, but these early efficiencies are approaching parity with B-doped cells.

**Table 9.3 Average and best cell efficiency of PERC cells from In-doped set A and b-doped sets B and C.**

| Set | Dopant Type | | $V_{oc}$ (mV) | $J_{sc}$ (mA/cm$^2$) | FF (%) | η (%) |
|---|---|---|---|---|---|---|
| A | Indium | Best | 653 | 38.9 | 78.7 | 20 |
| | | Avg(6) | 647 | 38.7 | 78.7 | 19.7 |
| B | Boron | Best | 667 | 38.6 | 79.6 | 20.5 |
| | | Avg(9) | 665 | 38.5 | 79.4 | 20.3 |
| C | Boron | Best | 662 | 38.7 | 78.8 | 20.2 |
| | | Avg(6) | 662 | 38.6 | 78.6 | 20.1 |

The noted gap in In- and B-doped PERC cell performance is primarily due to lower $V_{oc}$. Initial experiment on bulk lifetime, IQE (Figure 9.2) and LBIC (Figure 9.3) of three representative cells indicate that this is proportional to slightly lower effective bulk lifetime ($\tau_{eff}$) in the In-doped devices. In-doped wafers had effective bulk lifetime of 170 μs, compared to 600 μs and 320 μs for Sets B and C. PC1D modeling (Table 9.4) showed an excellent match between the experimental and modeled I-V and IQE data at the measured lifetimes. Research is underway to identify the reason for and bridge this gap in effective lifetime in the In and B wafers by improving both the bulk properties and cell processing conditions.

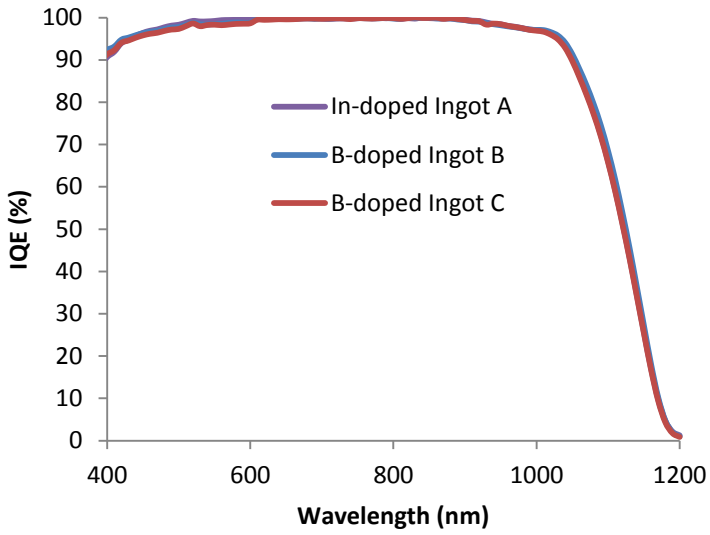



**Figure 9.2 IQE measurements of cells on In-doped Set A, B-doped Set B and Set C.**

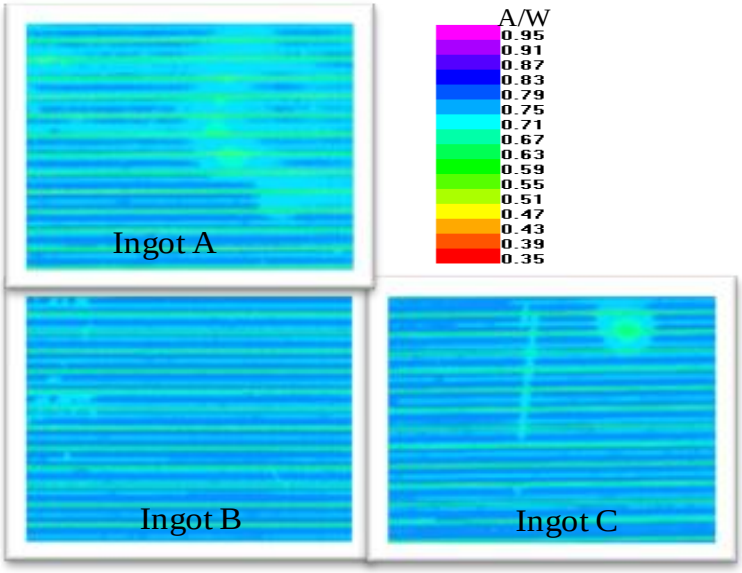



**Figure 9.3 LBIC images of the In-doped Set A (top left), B-doped Set B (bottom left) and Set C (bottom right).**

**Table 9.4 PC1D modeling parameters of the 20.0% In-doped PERC cell (set A), 20.4% B-doped PERC cell (set B), and 20.2% PERC cell (set C).**

| Cell Parameters | In-doped (set A) | B-doped (set B) | B-doped (set C) |
|---|---|---|---|
| Wafer thickness (μm) | 180 | 180 | 180 |
| Base Resistivity (Ω-cm) | 3.1 | 1.5 | 2.7 |
| $R_{SERIES}$ (Ω-cm$^2$) | 0.5 | 0.5 | 0.5 |
| $R_{SHUNT}$ (Ω-cm$^2$) | 41667 | 41667 | 41667 |
| $n_2$ | 2.1 | 2.1 | 2.1 |
| $J_{02}$ (nA/cm$^2$) | 25 | 25 | 25 |
| Emitter sheet resistance(Ω/sq) | 95 | 95 | 95 |
| Junction Depth (μm) | 0.31 | 0.31 | 0.31 |
| Surface concentration (cm$^{-3}$) | 1.3E+20 | 1.3E+20 | 1.3E+20 |
| Texture angle (degrees) | 54.74 | 54.74 | 54.74 |
| Texture depth (μm) | 3.535 | 3.535 | 3.535 |
| Rear surface charge (cm$^{-2}$) | 2.2E+11 | 2.2E+11 | 2.2E+11 |
| $t_{bulk}$ (μs) | 170 | 600 | 320 |
| BSRV (cm/s) | 100 | 100 | 100 |
| FSRV (cm/s) ) | 10000 | 10000 | 10000 |
| $R_{back}$ (%) | 95 | 95 | 95 |
| Grid shading (%) | 6.5 | 6.5 | 6.5 |
| Modeled $V_{OC}$ (mV) | 652 | 663 | 658 |
| Modeled $J_{SC}$ (mA/cm$^2$) | 38.7 | 38.9 | 38.9 |
| Modeled FF (%) | 79.3 | 79.3 | 78.9 |
| Modeled Efficiency (%) | 20.0 | 20.4 | 20.2 |

### 9.3.4 LID Effect on In- and B-Doped PERC Cells

Table 9.5 shows the impact of LID on the PERC cells made on three types of substrates. It is interesting that virtually no LID was observed in the In-doped PERC cells. However, B-doped PERC cell (Set B) showed a drop in cell efficiency from 20.4% to 19.4%. This huge drop in efficiency is consistent with the high oxygen concentration (21 ppma) in this set. B-doped set C with 14 ppma oxygen showed a LID induced decrease in efficiency from 20.1% to 19.5%. As expected, the LID effect is greater in the B-doped PERC cells compared with the baseline full Al-BSF cells. It is important to note that in spite of slightly lower starting efficiency, the final stabilized efficiency of In-doped PERC cells after LID was decisively above that of the B-doped PERC cells by about 0.4% absolute.

**Table 9.5 Cell efficiency before and after LID on In-doped set A and B-doped sets B and C cells.**

| Ingot | Dopant Type | | $V_{oc}$ (mV) | $J_{sc}$ (mA/cm$^2$) | FF (%) | η (%) |
|---|---|---|---|---|---|---|
| A | Indium | Initial | 651 | 38.8 | 78.7 | 19.9 |
| | | LID | 650 | 38.8 | 78.4 | 19.8 |
| B | Boron | Initial | 667 | 38.6 | 79.3 | 20.4 |
| | | LID | 651 | 38.1 | 78.1 | 19.4 |
| C | Boron | Initial | 662 | 38.6 | 78.5 | 20.1 |
| | | LID | 652 | 38.5 | 77.4 | 19.5 |

## 9.4 Summary

This chapter demonstrates, for the first time, a 20% efficient large-area, screen-printed, In-doped, monocrystalline cell with no appreciable light light-induced

degradation. Conventional full Al-BSF baseline cells gave nearly identical efficiencies of ~19.1% for the In- and two B-doped sets. However, after ~0.7 sun, 72-hour illuminations, the In-doped cells showed negligible LID, resulting in highest stabilized efficiency. When building PERC structures, In-doped substrates gave a best efficiency of 20.0% compared with 20.3% and 20.5% for the two B-doped sets. However, after light exposure, a high oxygen (21 ppma) B-doped cell (set B) with efficiency of 20.4% showed ~1% absolute efficiency loss due to LID and a 20.1% cell (set C) with 14 ppma oxygen dropped by ~0.6% due to LID. In contrast, an indium-doped cell showed only a loss of ~0.1% due to LID. Thus, despite slightly lower starting efficiency, In-doped PERC cells showed much higher stabilized efficiency compared to their counterpart B-doped PERC cells. This shows the potential of In-doped cells for higher stabilized efficiency and energy production over a module's service period.

# CHAPTER 10

# GUIDELINES FOR FUTURE WORK

This thesis developed a cost-effective, simple, and manufacturable process sequence to fabricate high-efficiency screen-printed PERC cells on industrial grade 239 $cm^2$ p-type Cz Si wafers using commercial ready technologies and equipment. This innovative low-cost process sequence features ion-implanted emitter, single high-temperature anneal step, optimized dielectric surface passivation, AR coating, rear reflector, fine line screen-printed metallization on front, and optimized line contact geometries on the back side. The PERC cells fabricated with this process achieved 20.8% efficiency on commercial grad 239 $cm^2$ Cz silicon wafers compared to 18.3% industrial type full Al-BSF cells at the start of this thesis. We also developed a roadmap to attain 21% efficiency at the start of this research. Thus there is still 0.2% efficiency gap between the PERC cell achieved in this research and the roadmap efficiency target of 21%. Therefore, this chapter suggests research directions that can further improve the cell design to attain higher efficiency. Figure 10.1 shows a new and practical technology roadmap for driving the efficiency of our PERC cells from 20.8% to 22% by three additional technology developments (1) use of selective emitter (150/85 Ω/sq) in conjunction with fine line double printing technology which can print ~40 μm lines, (2) use of low resistivity (1 Ω-cm) and high lifetime (~2 ms) silicon wafer, and (3) higher quality passivation layers (BSRV ~10 cm/s and FSRV ~2000 cm/s) on back and front sides. The first technology innovation will increase the efficiency from 20.85 to 21.1%, second will drive it to 21.3% and the third innovation can push the efficiency of PERC cell to 22% (Figure 10.1).

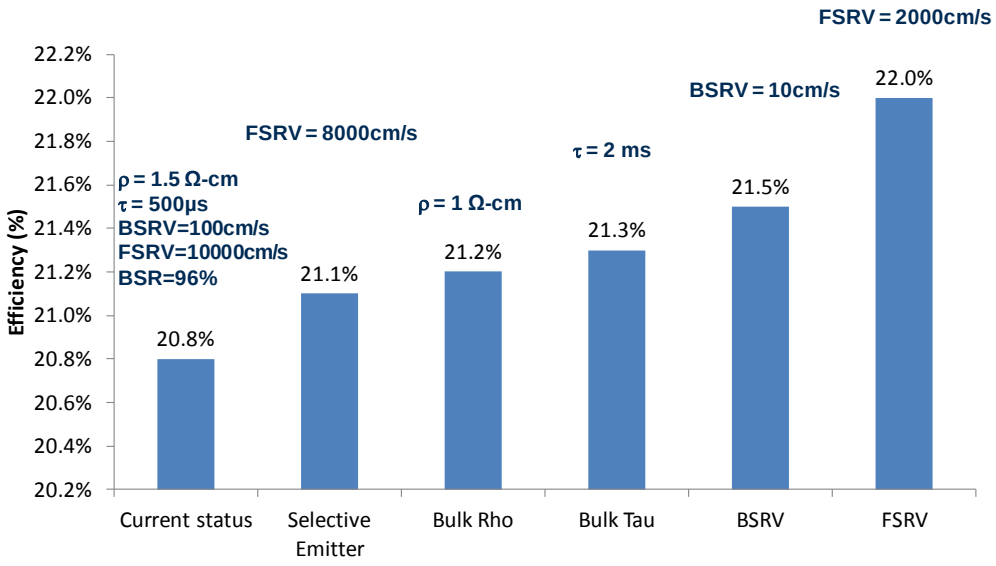



**Figure 10.1 Technology roadmap to achieve 22% efficient PERC solar cells.**

## 10.1 Selective Emitter with Fine Line Double Printing Technology

In the phase-I of this research, ion implantation was used successfully to form the selective emitter to achieve GEN-I screen-printed PERC cell efficiency of 20.2% (Chapter 7). Selective emitter improved cell efficiency by reducing emitter recombination and contact resistance simultaneously. In the phase-II of this research, we switched from the selective emitter (100/50 Ω/sq) to a high sheet resistance homogeneous emitter (~90 Ω/sq) to simplify the process sequence and attain higher efficiency. We were successful in making good ohmic contacts to this high sheet resistance homogeneous emitter using the new DuPont PV17S Ag paste. These findings indicate an opportunity to develop a more lightly doped selective emitter with a 150/90 Ω/sq emitters to further reduce the FSRV and emitter bulk recombination $J_{oe}$ while maintaining good ohmic contact on ~90Ω/sq selective region which could lead to ≥ 21%-efficient PERC cells. In addition to the selective emitter, double printing technology can lead to line width approaching 40 μm. In double printing, a thin and narrow seed layer is printed first followed by a second

print to build the line height resulting in higher aspect ratio and reduced shading. In order to take full benefit of these two innovative technologies (lowly doped selective emitter and double print), we need to optimize the design of the front grid. Next section shows the results of a simple analytical model that was developed in this thesis to optimize the front grid for this purpose and calculate the efficiency enhancement.

### 10.1.1 Development of an Analytical Model for Optimizing Front Grid Design for High Sheet Resistance Selective Emitter PERC Cell

Simple analytical model for optimizing grid pattern was developed, which first calculates all the components of the series resistance based on the experimentally measured parameters of a reference cell. After that, components of $R_s$ are calculated for different finger spacing/number of fingers using the analytical model to obtain the new $R_s$ value for each spacing. Then this $R_s$ is used to calculate the FF. $J_{sc}$ and $V_{oc}$ values are calculated from metal fraction. $J_{sc}$ is assumed to be a linear function of metal coverage (Equation (10.1)). $J_o$ is calculated from the front and back metal coverage as well as $J_o$ components from the field region (Equation (10.2)). $V_{oc}$ is then calculated from $J_{sc}$ and $J_o$. Finally, cell efficiency is calculated from $J_{sc}$, $V_{oc}$, and FF as a function of finger spacing.

#### 10.1.1.1 Determination of Components of $R_s$ for Different Finger Spacing or Number of Fingers

We utilized the Meier's methodology from reference [130, 131] to calculate components of $R_s$ based on experimentally measured parameters from the cell. Figure 10.2 shows a diagram for the cell with a three-busbar pattern used in this study. The full cell size is 156 mm×156 mm. The unit cell used for the analysis has length of 2.6 cm (a),

width of 1.04 cm (2nb), and finger spacing of 0.173 cm (2b). The current pick-up probes to contact busbar in our light IV tester are separated by 1 cm.

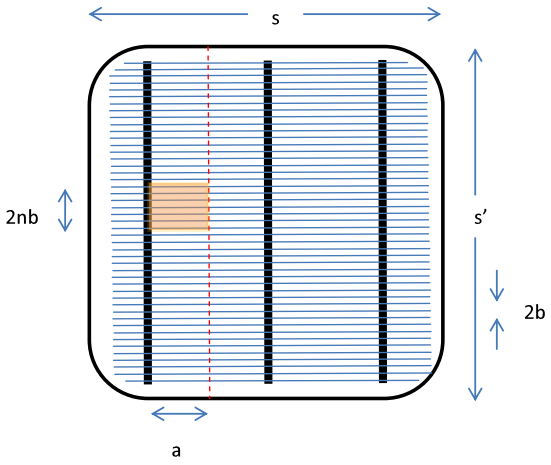



**Figure 10.2 Diagram of an industrial cell with three-busbar H pattern. Orange color in the diagram represents the unit cell for the analysis.**

In this study, we analyzed a 20.6% PERC cell with ~70 µm wide Ag fingers in combination with ion implanted ~90 Ω/sq homogeneous emitter. The expressions used to calculate various $R_s$ components are summarized in Table 10.1 while the measured parameters are summarized in Table 10.2.

**Table 10.1 Analytical expression of the series resistance components for a GEN-II PERC cell.**

| Component | Expression | Value (Ω-cm$^2$) |
|---|---|---|
| Busbar | $R_s(busbar) = (1/3)a(n+1)(n+2)b^2(2R_{bus}/s')$ | 0.0054 |
| Gridlines | $R_s(gridlines) = (2/3)(abn_{gl})BBR$ | 0.3677 |
| Emitter sheet | $R_s(sheet) = (1/3)b^2R_{sheet}$ | 0.2128 |
| Substrate | $R_s(substrate) = \rho_w t_w$ | 0.0360 |
| Front contact resistance | $R_s(front\ contact) = \rho_{fc}/f_{fm}$ | 0.0916 |
| Back contact resistance | $R_s(back\ contact) = \rho_{bc}/f_{bm}$ | 0.0640 |
| Total series resistance (from PFF and FF) | $R_s(total) = [V_{oc}/J_{sc}][(PFF-FF)/PFF]$ | 0.7775 |

**Table 10.2 Experimentally measured parameters for a 20.6% PERC cell.**

| Parameter | Description | Value | Unit |
|---|---|---|---|
| $n_{bb}$ | number of bus bars | 3 | |
| a | length of grid line per unit cell | 2.6 | cm |
| 2b | grid line spacing | 0.173 | cm |
| n | grid lines per unit cell | 6 | |
| $n_{gl}$ | total grid lines (vary) | 89 | |
| l | total length of grid line | 15.6 | cm |
| w | the grid line width | 0.007 | cm |
| 2w' | width of front busbar on cell | 1.5 | mm |
| $R_{sheet}$ | emitter sheet resistance | 90 | Ω/sq |
| $R_{sheet}$(metal) | back metal sheet resistance | 0.0264 | Ω/sq |
| ρ | wafer resistivity | 2 | Ω-cm |
| $t_w$ | wafer thickness | 0.018 | cm |
| BBR | Bus bar to bus bar resistance | 0.055 | Ω |
| $R_{bus}$ | Bus bar resistance | 0.1798 | Ω |
| $J_{sc}$ | $J_{sc}$ measured by cell tester | 0.0391 | $A/cm^2$ |
| $V_{oc}$ | $V_{oc}$ measured by cell tester | 0.664 | V |
| FF | FF measured by cell tester | 0.792 | |
| $R_s$ | series resistance measured by cell tester | 0.71 | $Ω\text{-}cm^2$ |
| $R_{sh}$ | shunt resistance measured by cell tester | 544923 | $Ω\text{-}cm^2$ |
| n | Ideality factor | 1.08 | |
| Efficiency | efficiency measured by cell tester | 20.6 | % |
| pseudo FF | pseudo FF measured by Suns-$V_{oc}$ | 0.83 | |
| $J_{ob\text{-}pas}$ | $J_{ob}$ associated with passivated back surface | 80 | $fA/cm^2$ |
| $J_{ob\text{-}met}$ | $J_{ob}$ associated with metalized back surface | 450 | $fA/cm^2$ |
| $J_{oe\text{-}pas}$ | $J_{oe}$ associated with passivated emitter surface | 70 | $fA/cm^2$ |
| $J_{oe\text{-}met}$ | $J_{oe}$ associated with metalized emitter surface | 1296 | $fA/cm^2$ |
| $f_{bm}$ | fraction of back metal coverage | 8.0% | |
| $f_{fm}$ | fraction of front metal coverage | 6.9% | |

The total series resistance, $R_s$(total), was determined from the pseudo fill factor (PFF) using a Suns-$V_{oc}$ measurement. The busbar resistance, $R_s$(busbar), is measured by four-point probe at the opposite ends of the busbar. The gridline resistance, $R_s$(gridline), is determined from the measurement of resistance between adjacent busbars, busbar-to-

busbar resistance (BBR), which provides an average gridline resistance over the all $n_{gl}$ gridlines. The substrate resistance is measured by four-point probe. The front sheet resistance and front contact resistance are determined by TLM-like pattern, which was laser cut from the cell with 1 cm strip. Figure 10.3 shows the TLM-like measured data for a 20.6% PERC cell. The sheet resistance is determined by the slope of the regression line while the contact resistance is determined from the intercept. Once these $R_s$ components are determined, the back contact resistance can then be inferred by subtracting the sum of the components from the total series resistance.

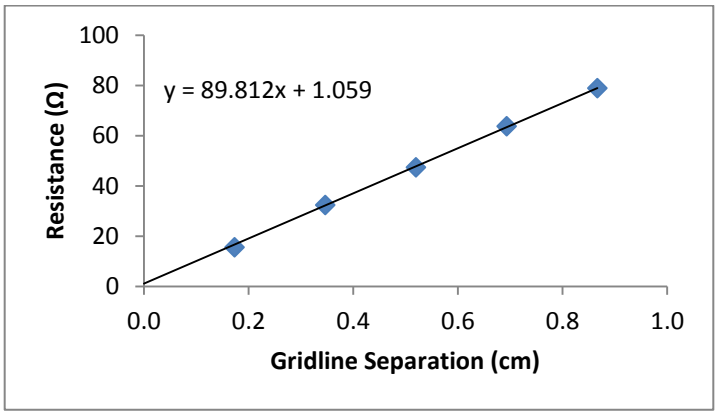



**Figure 10.3 Resistance data for determine sheet resistance and contact resistivity from TLM-like pattern for a 20.6% PERC cell.**

After the above parameters were determined for the reference cell, various components of $R_s$ for different finger spacing/number of fingers were calculated using this analytical model. The calculated results are summarized in Table 10.3.

**Table 10.3 Calculated $R_s$ and its corresponding component for different finger spacing or number of fingers.**

| Finger spacing (mm) | Number of fingers | Resistance ($\Omega$-cm$^2$) | | | | | |
|---|---|---|---|---|---|---|---|
| | | Busbar | Fingers | Contact | Emitter | Substrate | Total $R_s$ |
| 2.58 | 60 | 0.012 | 0.547 | 0.136 | 0.499 | 0.036 | 1.23 |
| 2.20 | 70 | 0.009 | 0.467 | 0.116 | 0.363 | 0.036 | 0.99 |
| 1.93 | 80 | 0.007 | 0.409 | 0.102 | 0.279 | 0.036 | 0.83 |
| 1.71 | 90 | 0.005 | 0.363 | 0.090 | 0.219 | 0.036 | 0.71 |
| 1.54 | 100 | 0.004 | 0.327 | 0.081 | 0.178 | 0.036 | 0.63 |
| 1.40 | 110 | 0.004 | 0.297 | 0.074 | 0.147 | 0.036 | 0.56 |
| 1.28 | 120 | 0.003 | 0.272 | 0.068 | 0.123 | 0.036 | 0.50 |
| 1.19 | 130 | 0.003 | 0.251 | 0.063 | 0.105 | 0.036 | 0.46 |
| 1.10 | 140 | 0.002 | 0.233 | 0.058 | 0.091 | 0.036 | 0.42 |
| 1.03 | 150 | 0.002 | 0.217 | 0.054 | 0.079 | 0.036 | 0.39 |

10.1.1.2 Determination of $J_{sc}$, $V_{oc}$, FF, and Efficiency as a Function of Finger Spacing

After determining the components of $R_s$, next step was to assess the impact of finger spacing on $J_{sc}$, $V_{oc}$ and FF in order to calculate the cell efficiency. As the spacing increases, $J_{sc}$ should increase because of reduced shading, $V_{oc}$ should increase because of reduced metal recombination, and FF should decrease because of increased series resistance. Therefore, we need to optimize the design of the grid to achieve maximum efficiency. In this study, we assumed $J_{sc}$ increases linearly with the uncovered area and can be expressed as follows:

$$J_{sc} = J_{sc0} + J_{sc0}(f_{fm0} - f_{fm}) \qquad (10.1)$$

where $J_{sc0}$ is the short current density of the reference cell, $f_{fm0}$ is fraction of front metal coverage of the reference cell, and $f_{fm}$ is front metal coverage of new screen printing technology. The total revere saturation current density $J_o$ can be obtained by:

$$J_0 = (f_{bm})J_{0b-met} + (1 - f_{bm})J_{0b-pas} + (f_{fm})J_{0e-met} + (1 - f_{fm})J_{0e-pas} \quad (10.2)$$

where $f_{bm}$ is the fraction of the rear surface covered with metal, $J_{ob\text{-}met}$ is the $J_0$ component associated with the metalized rear surface (taken to be 450 fA/cm$^2$ from [132]), $J_{ob\text{-}pass}$ is the $J_0$ component associated unmetallized rear surface (100 fA/cm$^2$ from our measurements), $J_{oe\text{-}metal}$ is the $J_0$ component associated with the metalized emitter surface (1296 fA/cm$^2$ from [113]), $J_{oe\text{-}pass}$ is the $J_0$ component associated unmetallized emitter surface (70 fA/cm$^2$ form our measurements). The $V_{oc}$ can now be obtained from the calculated $J_{sc}$ and $J_o$ values:

$$V_{oc} = \frac{kT}{q} \ln \left(\frac{J_{sc}}{J_0} + 1\right) \quad (10.3)$$

The FF is then calculated by the following equations:

$$FF_0 = \frac{v_{oc} - \ln (v_{oc} + 0.72)}{v_{oc} + 1}, \text{where } v_{oc} = \frac{qV_{oc}}{nkT} \quad (10.4)$$

$$R_{CH} = \frac{V_{oc}}{J_{sc}}, r_s = \frac{R_s}{R_{CH}}, \text{and } r_{sh} = \frac{R_{sh}}{R_{CH}} \quad (10.5)$$

$$FF_s = FF_0(1 - r_s) \quad (10.6)$$

$$FF = FF_s\left[1 - \frac{(v_{oc} + 0.7)FF_s}{v_{oc} r_{sh}}\right] \quad (10.7)$$

Once $J_{sc}$, $V_{oc}$, FF are calculated from the grid spacing, the cell efficiency can be obtained by:

$$\eta = \frac{V_{oc} J_{sc} FF}{P_{in}} \quad (10.8)$$

Using the above analytical model (equation (10.1) to (10.8)) and predetermined $R_s$ values (Table 10.3), the cell efficiency for various grid designs can be determined. Table 10.4 and Figure 10.4 summaries the result of these calculations and reveals the impact of

finger spacing on the cell efficiency. The predicted peak efficiency is 20.61% for 90 gridlines agrees very well with reference cell efficiency of 20.6% with 70 µm wide 89 gridlines.

**Table 10.4 Calculated $J_{sc}$, $V_{oc}$, FF and efficiency for different finger spacing based on the 20.6% reference cell with 70 µm wide fingers and a 90Ω/sq emitter.**

| Finger spacing (mm) | Number of fingers | Front metal coverage | $J_o$ (fA/cm$^2$) | $J_{sc}$ (mA/cm$^2$) | $V_{oc}$ (mV) | FF | η (%) |
|---|---|---|---|---|---|---|---|
| 2.58 | 60 | 5.6% | 278 | 39.6 | 665 | 0.770 | 20.28 |
| 2.20 | 70 | 6.0% | 284 | 39.4 | 664 | 0.782 | 20.48 |
| 1.93 | 80 | 6.5% | 290 | 39.3 | 664 | 0.789 | 20.57 |
| 1.71 | 90 | 6.9% | 297 | 39.1 | 663 | 0.795 | 20.61 |
| 1.54 | 100 | 7.4% | 303 | 38.9 | 662 | 0.800 | 20.60 |
| 1.40 | 110 | 7.8% | 310 | 38.7 | 662 | 0.803 | 20.58 |
| 1.28 | 120 | 8.3% | 316 | 38.5 | 661 | 0.806 | 20.53 |
| 1.19 | 130 | 8.7% | 323 | 38.4 | 661 | 0.808 | 20.47 |
| 1.10 | 140 | 9.2% | 329 | 38.2 | 660 | 0.809 | 20.40 |
| 1.03 | 150 | 9.6% | 336 | 38.0 | 659 | 0.811 | 20.32 |

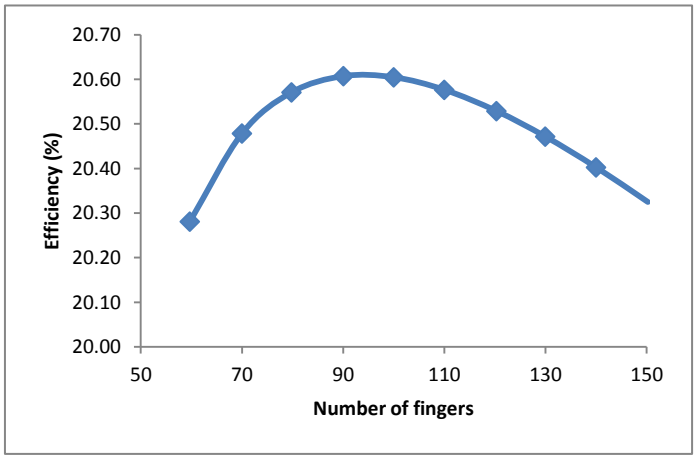



**Figure 10.4 Calculated efficiency as a function of number of 70 µm wide fingers for the reference PERC cell ($V_{oc}$ = 664mV, $J_{sc}$ = 39.1 mA/cm$^2$, FF = 79.2%, η = 20.6% with 70 µm wide fingers and a 90 Ω/sq emitter)**

### 10.1.1.3 Modeling the Efficiency Enhancement from Lightly Doped Selective Emitter and Fine Line Double Printing Technology

The analytical model developed in the previous section was used to assess the efficiency enhancement from 150/90 Ω/sq selective emitter and 40 µm lines. Figure 10.5 shows the calculated efficiency as a function of number of fingers and finger width. The double printed Ag grid height was assumed to be ~40 µm (twice that of the 20.6% reference cell). Figure 10.5 shows that there is a different optimum number of fingers for each line width. In addition, the peak efficiency increases with the decreases in the line width and reaches 21.1% for 40 µm line width with 130 gridlines. This is a good topic for future work to attain ~0.3% absolute efficiency gain.

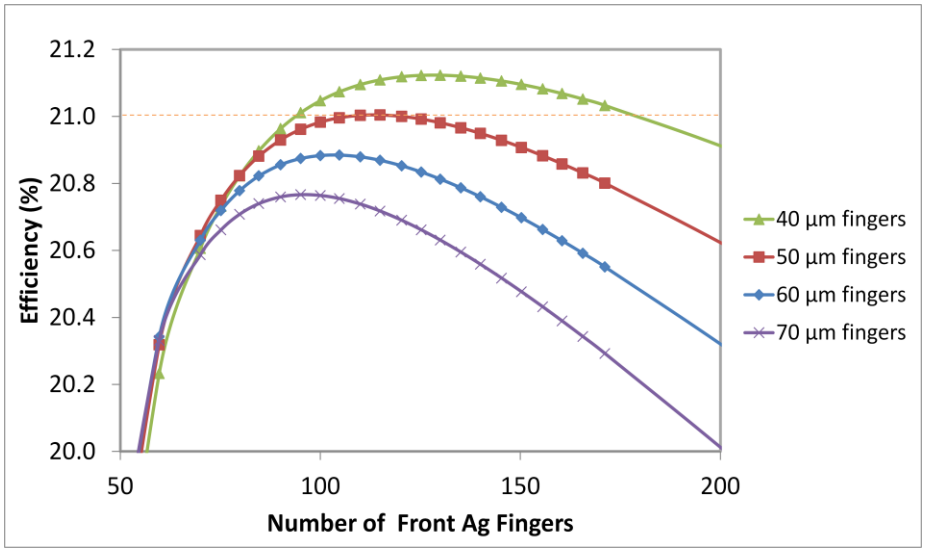



**Figure 10.5 Efficiency as a function of finger width and number of fingers for a combination of a 150/90 Ω selective emitter and double printing technology.**

## 10.2 Lower Resistivity and Higher Lifetime Substrates for High Efficiency PERC Si Solar Cells

After matching the 20.8% efficiency by PC1D modeling (Table 8.8), we extended the model calculations to find what other material and device performance can be optimized for efficiency gain. Figure 10.6 shows that 0.2-0.3 % efficiency enhancement can be achieved over our 20.8% PERC cell by reducing the base resistivity from 1.5 Ω-cm to ~1 Ω-cm in combination with 2 ms bulk lifetime (Figure 10.7). There are two challenges in this approach. First, it is difficult to achieve 2 ms bulk lifetime in Cz material and secondly lower resistivity will lead to higher LID [124], unless In-doped or low oxygen wafers are used.

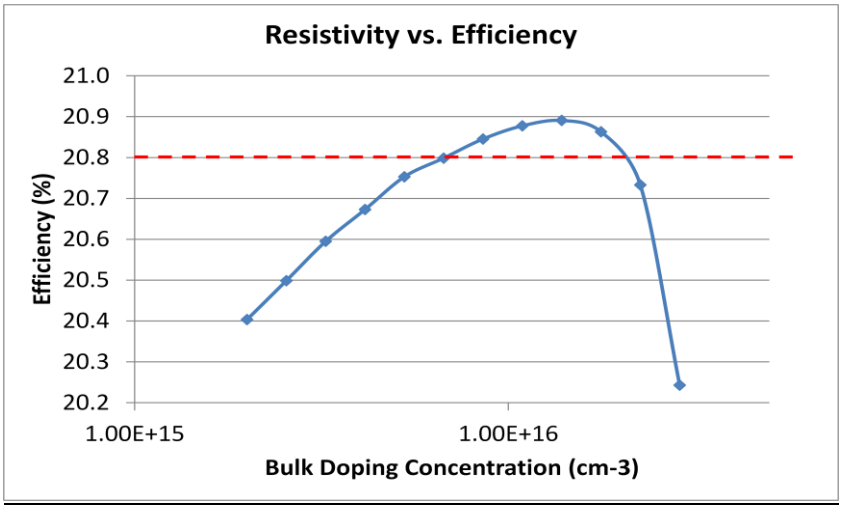



**Figure 10.6 PERC cell efficiency as a function bulk doping concentration for bulk lifetime of 500 µs.**

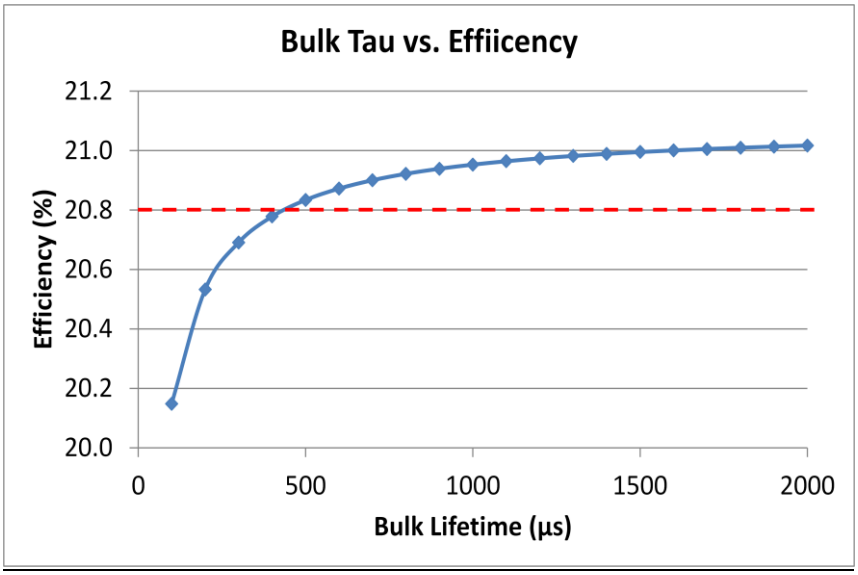



**Figure 10.7 PERC cell efficiency as a function of bulk lifetime in 1 Ω-cm Si substrate.**

## 10.3 Higher Quality Dielectric Passivation for Higher Efficiency PERC Cells

The third enhancement in efficiency over our 20.8% PERC cells can be realized by further reducing the FSRV and BSRV with higher quality surface passivation layers. PC1D modeling in Figure 10.8 and Figure 10.9 show that reduced FSRV and BSRV can provide 0.1-0.4% efficiency enhancement over our 20.8% cell. Very low SRV of 13 cm/s on p-type Si with 20 nm thick ALD $Al_2O_3$ and a SRV of 2 cm/s on n-type Si with 26 nm thick $Al_2O_3$ have been reported recently [69]. This excellent passivation is attributed to the presence of high negative fixed charges ($Q_f \sim 10^{12}–10^{13}$ $cm^{-2}$) in $Al_2O_3$ in combination with a low density of interface states ($D_{it}$).

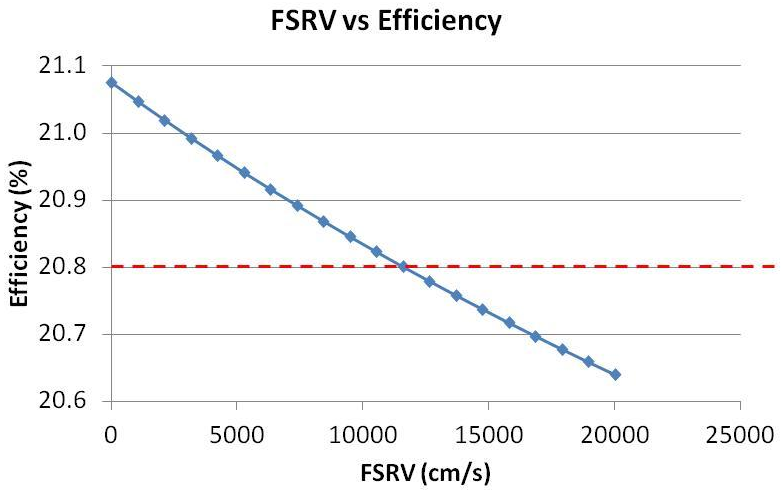



**Figure 10.8 Efficiency as a function of FSRV on the PERC cell (BSRV = 100 cm/s).**

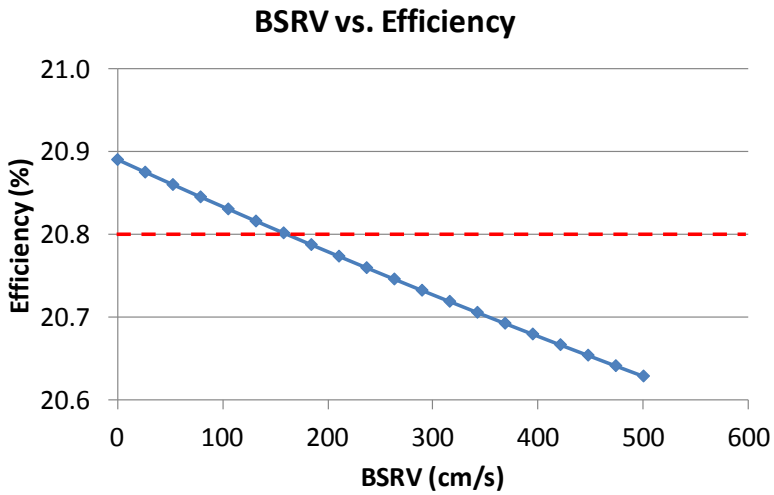



**Figure 10.9 Efficiency as a function of BSRV (FSRV = 10,000cm/s).**

The above recommendations for future research are supported by PC1D modeling in Table 10.5. It shows the modeling of 20.8% PERC cell fabricated in this research along with target efficiencies with future technology developments. This table also lists PC1D modeling parameters of a record high 24.5% 4 $cm^2$ PERL cell [21] for comparison.

The modeling results show that the integration of above technology enhancements could result in 22% efficient screen printed PERC cells on commercial grade Cz Si wafers. Use of lightly doped selective emitter and fine line double printing can raise the efficiency to 21.1% and use of lower resistivity high lifetime wafers with improved front and back dielectric passivation can drive efficiency to 22%. Device modeling in Table 10.5 shows that the major difference between the 22% PERC cell at this stage and the laboratory PERL cell is the primarily photolithography contacts used in the 24.5% laboratory cell which led to significantly reduced shading loss (1%) and FSRV (1000 cm/s) and excellent contacts with 83% FF on 200 Ω/sq emitter. These cannot be achieved with current screen printing technology.

**Table 10.5 PC1D modeling parameters for the 20.8% PERC and 24.5% PERL cells and a roadmap to 22% efficiency by future research and development.**

| Cell Parameters | 20.8% Current | 21.1% Future | 22.0% Future | 24.5% PERL |
|---|---|---|---|---|
| Wafer thickness (µm) | 180 | 180 | 180 | 370 (+0.1%) |
| Base Resistivity (Ω-cm) | 2.0 | 2.0 | 1.0 | 1.0 |
| RSERIES (Ω-cm2) | 0.6 | 0.6 | 0.6 | 0.3 (+0.4%) |
| $R_{SHUNT}$ (Ω-cm$^2$) | 41667 | 41667 | 41667 | 41667 |
| $N_2$ | 2.2 | 2.2 | 2.2 | NA(+0.4%) |
| $J_{02}$ (nA/cm$^2$) | 20 | 20 | 20 | NA |
| Emitter sheet resistance(Ω/sq) | 90 | 150 | 150 | 200 |
| Junction Depth (µm) | 0.35 | 0.30 | 0.30 | 1.0 |
| Surface concentration (cm$^{-3}$) | 2.0E+20 | 7.4E+19 | 7.4E+19 | 5.7E+18 |
| Texture angle (degrees) | 54.74 | 54.74 | 54.74 | 54.74 |
| Texture depth (µm) | 3.535 | 3.535 | 3.535 | 3.535 |
| Rear surface charge (cm$^{-2}$) | 2.2E+11 | 2.2E+11 | 2.2E+11 | 2.2E+11 |
| $t_{bulk}$ (µs) | 500 | 500 | 2000 | 2000 |
| BSRV (cm/s) | 100 | 100 | 10 | 15 |
| FSRV (cm/s) | 10000 | 8000 | 2000 | 1000 (+0.5%) |
| $R_{back}$ (%) | 96 | 96 | 96 | 98 (+0.1%) |
| Grid shading (%) | 6.3 | 5.5 | 5.5 | 1.0 (+1.0%) |
| Modeled $V_{OC}$ (mV) | 665 | 672 | 692 | 704 |
| Modeled $J_{SC}$ (mA/cm$^2$) | 39.2 | 39.4 | 39.6 | 41.9 |
| Modeled FF (%) | 79.8 | 79.8 | 80.3 | 83.0 |
| Modeled Efficiency (%) | 20.8 | 21.1 | 22.0 | 24.5 |

# REFERENCES


[1] U. S. E. I. A. Annual Energy Review 2011, Report number DOE/EIA-0384, 2012.

[2] S. Stoft. (2012). *Global Warming- Evidence that CO2 is Cause*. Available: http://zfacts.com/p/226.html

[3] NASA. *Global Horizontal Radiation*. Available: https://eosweb.larc.nasa.gov/cgi-bin/sse/global.cgi?

[4] I. E. Agency, "Energy Technology Perspectives 2010- Scenarios and Strategies to 2050," 2010.

[5] C. Xin, C. Pan, Y. Liu, and Z. L. Wang, "Hybrid cells for simultaneously harvesting multi-type energies for self-powered micro/nanosystems," *Nano Energy*, vol. 1, pp. 259-272, 2012.

[6] S. E. I. Associaiton, "Solar Market Insight Report 2012 Year in Review," 2012.

[7] M. H. Kang, "Development of high-efficiency silicon solar cells and modeling the impact of system parameters on levelized cost of electricity," Ph.D. Thesis, Georgia Institute of Technology, 2013.

[8] D. D. C. Smith, P.J. ; Masad, A. ; Waldhauer, A. ; Westerberg, S. ; Johnson, M. ; Xiuwen Tu ; Dennis, T. ; Harley, G. ; Solomon, G. ; Seung Rim ; Shepherd, M. ; Harrington, S. ; Defensor, M. ; Leygo, A. ; Tomada, P. ; Junbo Wu ; Pass, T. ; Ann, L. ; Smith, L. ; Bergstrom, N. ; Nicdao, C. ; Tipones, P. ; Vicente, D., "Generation III high efficiency lower cost technology: transition to full scale manufacturing," in *38th IEEE Photovoltaic Specialists Conference*, Austin, TX, 2012, pp. 001594 - 001597.

[9] D. I. Fujishima, H. ; Tsunomura, Y. ; Asaumi, T. ; Taira, S. ; Kinoshita, T. ; Taguchi, M. ; Sakata, H. ; Maruyama, E., "High-performance HIT solar cells for thinner silicon wafers," in *35th IEEE Photovoltaic Specialists Conference*, Honolulu, HI, 2010, pp. 003137 - 003140.

[10] A. W. Blakers, A. Wang, A. M. Milne, J. Zhao, and a. M. A. Green, "22.8% efficient silicon solar cell," *Applied Physics Letters*, vol. 55, pp. 1363-1365, 1989.

[11] A. Rohatgi, A. Ristow, A. Das, and S. Ramanathan, "Road to Cost Effective Silicon PV," in *18th International Photovoltaic Science and Engineering Conference*, Kolkata, India, 2009.

[12] G. Hahn, "Status of Selective Emitter Technologies," in *25th European Photovoltaic Solar Energy Conference and Exhibition/5th World Conference on Photovoltaic Energy Conversion*, Valencia, 2010.

[13] V. Meemongkolkiat, "Development of high efficiency monocrystalline si solar cells through improved optical and electrical confinement," Ph.D., School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, 2008.

[14] X. Chen, K. Church, H. Yang, I. B. Cooper, and A. Rohatgi, "Improve Front Side Metallizaiton for Silicon Solar Cells By Direct Printing," in *37th IEEE Photovoltaic Specialists Conference*, Seattle, 2011, pp. 3667-3671.

[15] J.-H. Lai, I. B. Cooper, X. Chen, K. Church, H. Yang, and A. Rohatg, "Large-area ~20% efficient silicon solar cells using fine line direct printing," in *38th IEEE Photovoltaic Specialists Conference*, Austin, Texas, 2012, pp. 002192-002195.

[16] W. Shockley and W. T. Read, "Statistics of the Recombinations of Holes and Electrons," *Physical Review,* vol. 87, pp. 835–842, 1952.
[17] M. A. Green, *Solar Cells: Operating Principles, Technology and System Applications*: University of New South Wales, 1986.
[18] A. Goetzberger, J. Knobloch, and B. Voss, *Crystalline Silicon Solar Cells*: Wiley;, 1998.
[19] *Optical Properties of Silicon*. Available: http://pveducation.org/pvcdrom/materials/optical-properties-of-silicon
[20] D. L. Meier, E. A. Good, R. A. Garcia, B. L. Bingham, S. Yamanaka, V. Chandrasekaran, and C. Bucher, "Determining Components of Series Resistance from Measurements on a Finished Cell," in *IEEE 4th World Conference on Photovoltaic Energy Conversion*, Waikoloa, HI, 2006, pp. 1315 - 1318.
[21] A. G. Aberle, *Crystalline Silicon Solar Cells: Advanced Surface Passivation and Analysis*. Centre for Photovoltaic Engineering: University of New South Wale, 1999.
[22] H. Schlangenotto, H. Maeder, and W. Gerlach, "Temperature dependence of the radiative recombination coefficient in silicon," *Physica Status Solidi A,* vol. 21, pp. 357-367, 1974.
[23] J. Dziewior and W. Schmid, "Auger Coefficients for Highly Doped and Highly Excited Silicon," *Applied Physics Letters,* vol. 31, pp. 346-348, 1977.
[24] R. N. Hall, "Electron-Hole Recombination in Germanium," *Phycical Review,* vol. 87, pp. 387-387, 1952.
[25] F. Montillo and P. Balk, "High Temperature Annealing of Oxidized Silicon Surfaces," *J. Electrochem. Soc.,* vol. 118, pp. 1463-1468, 1971.
[26] S. Dauwe, L. Mittelstadt, A. Metz, and R. Hezel, "Experimental evidence of parasitic shunting in silicon nitride rear surface passivated solar cells," *Progress in Photovoltaics,* vol. 10, pp. 271-278, 2002.
[27] R. A. Sinton, Y. Kwark, J. Y. Gan, and R. M. Swanson, "27.5-Percent Silicon Concentrator Solar Cells," *IEEE ELECTRON DEVICE LETTERS,* vol. 7, pp. 567- 569, 1986.
[28] D. De Ceuster, P. Cousins, D. Rose, M. Cudzinovic, and W. Mulligan, "Low cost, high volume production of >22% efficiency silicon solar cells," in *22nd European Photovoltaic Specialist Conference*, Milan, Italy, 2007, pp. 816-819.
[29] P. J. Cousins, D. D. Smith, H.-C. Luan, J. Manning, T. D. Dennis, A. Waldhauer, K. E. Wilson, G. Harley, and W. P. Mulligan, "Generation 3: Improved performance at lower cost," in *35th IEEE Photovoltaic Specialists Conference*, Hawai, USA, 2010, pp. 275-278.
[30] W. P. Mulligan, D. H. Rose, M. J. Cudzinovic, D. M. D. Ceuster, K. R. McIntosh, D. D. Smith, and R. M. Swanson, "Manufacture of solar cells with 21% efficiency," in *19th European Photovoltaic Solar Energy Conference*, 2004, pp. 387-390.
[31] D. Fujishima, H. Inoue, Y. Tsunomura, T. Asaumi, S. Taira, T. Kinoshita, M. Taguchi, H. Sakata, and E. Maruyama, "High-performance HIT solar cells for thinner silicon wafers," in *35th IEEE Photovoltaic Specialists Conference*, Hawaii, USA, 2010, pp. 3137-3140.

[32] M. Taguchi, Y. Tsunomura, H. Inoue, S. Taira, T. Nakashima, T. Baba, H. Sakata, and E. Maruyama, "High-efficiency HIT solar cell on thin (<100 μm) silicon wafer," in *24th European Photovoltaic Solar Energy Conference*, Hamburg, Germany, 2009, pp. 1690-1693.

[33] P. Corporation. (2013). *Panasonic HIT® solar cell achieves world's highest conversion efficiency of 24.7% at research level*. Available: http://panasonic.co.jp/corp/news/official.data/data.dir/2013/02/en130212-7/en130212-7.html

[34] A. W. Blakers, A. Wang, A. M. Milne, J. Zhao, and M. A. Green, "22.8% efficient silicon solar cell," *Applied Physics Letters*, vol. 55, pp. 1363-1365, 1989.

[35] J. Zhao, A. Wang, and M. A. Green, "24.5% efficiency silicon PERT cells on MCZ substrates and 24.7% efficiency PERL cells on FZ substrates," *Progress in Photovoltaics: Research and Applications*, vol. 7, pp. 471-4, 1999.

[36] M. A. Green, "The path to 25% silicon solar cell efficiency: History of silicon cell evolution," *Prog. Photovolt: Res. Appl.*, vol. 17, pp. 183-189, 2009.

[37] A. Mohr, P. Engelhart, C. Klenke, S. Wanka, A. A. Stekolnikov, M. Scherff, S. Tardon, T. Rudolph, M. Hofmann, F. Stenzel, J. Lee, S. Diez, J. Wendt, W. Brendle, S. Schmidt, J. W. Müller, P. Wawer, M. Hofmann, P. Saint-Cast, J. Nekarda, D. Erath, J. Rentsch, and R. Preu, "20%-efficient rear side passivated solar sells in pilot series designed for conventional module assembling," presented at the 26th European Photovoltaic Solar Energy Conference, Hamburg, Germany, 2011.

[38] Z. Wang, P. Han, H. Lu, H. Qian, L. Chen, Q. Meng, N. Tang, F. Gao, Y. Jiang, J. Wu, W. Wu, H. Zhu, J. Ji, Z. Shi, A. Sugianto, L. Mai, B. Hallam, and S. Wenham, "Advanced PERC and PERL production cells with 20.3% record efficiency for standard commercial p-type silicon wafers," *Prog. Photovolt: Res. Appl.*, vol. 20, pp. 260–268, 2012.

[39] T. Dullweber, M. Siebert, B. Veith, C. Kranz, J. Schmidt, R. Brendel, B. F. P. Roos, T. Dippell, A. Schwabedissen, and S. Peters, "High-efficiency industrial-type PERC solar cells applying ICP AlOx as rear passivation layer," in *27th European Photovoltaic Solar Energy Conference*, Frankfurt, Germany, 2012, pp. 672 - 675.

[40] K. A. Mu¨nzer, J. Scho¨ne, A. Teppe, R. E. Schlosser, M. Hein, D. Hammer, S. Hu¨ls, M. Hanke, S. Keller, and P. Fath, "Advanced rear side technology for industrial high efficiency solar cells," in *25th European Photovoltaic Solar Energy Conference*, Valencia, Spain, 2010, pp. 2314–2318.

[41] T. Bo¨scke, R. Hellriegel, T. Wu¨therich, L. Bornschein, A. Helbig, R. Carl, M. Dupke, D. Stichtenoth, T. Aichele, R. Jesswein, T. Roth, C. Scho¨llhorn, T. Geppert, A. Grohe, J. Lossen, and H.-J. Krokoszinski, "Fully screen-printed PERC cells with laser-fired contacts—an industrial cell concept with 19.5% efficiency," in *37th IEEE Photovoltaic Specialists Conference*, Seattle, USA, 2011, pp. 3663–3666.

[42] J.-H. Lai, A. Upadhyaya, R. Ramanathan, A. Das, K. Tate, V. Upadhyaya, A. Kapoor, C.-W. Chai-Chen, and A. Rohatgi, "Large area 19.4% efficient rear passivated silicon solar cells with local Al BSF and screen-printed contacts," in *37th IEEE Photovoltaic Specialists Conference*, Seattle, USA, 2011, p. 1929.

[43] M. Osborne. (2014). *ISFH partnership pushes industrial PERC solar cell to record 21.2% efficiency*. Available: http://www.pv-tech.org/news/isfh_partnership_pushes_industrial_perc_solar_cell_to_record_21.2_efficienc

[44] S. Solar. (2013). *SCHOTT Solar and SCHMID Group lift PERC efficiency records to values of up to 21%*. Available: http://www.schmid-group.com/en/press-corner-news/press-releases/p107/schott-solar-and-schmid-lift-perc-efficieny-to-up-to-21.html

[45] B. Thaidigsmann, M. Linse, A. Wolf, F. Clement, D. Biro, and R. Preu, "The path to industrial production of highly efficient metal wrap through silicon solar cells," *Green,* vol. 2, pp. 171-176, 2013.

[46] J. Wu, Y. Liu, X. Wang, and L. Zhang, "Application of ion implantation emitter in PERC solar cells," *IEEE Journal of Photovoltaics,* vol. 4, pp. 52 - 57, 2014.

[47] H. Antoniadis, "Silicon ink high efficiency solar cells," in *34th IEEE Photovoltaics Specialists Conference*, Philadelphia, USA, 2009, pp. 650-654.

[48] H. Antoniadis, F. Jiang, W. Shan, and Y. Liu, "All screen printed mass production silicon ink selective emitter solar cells," in *35th IEEE Photovoltaic Specialists Conference*, Honolulu, USA, 2010, pp. 1193-1196.

[49] A. Esturo-Breton, F. B. Masouleh, M. Breselge, T. Friess, M. Geiger, E. Holbig, J. Isenberg, S. Keller, T. Kühn, J. Maier, A. Münzer, R. Schlosser, A. Schmid, C. Voyer, P. Winter, K. Bayer, J. Krümberg, S. Henze, I. Melnyk, M. Schmidt, S. Klingbeil, F. Walter, R. Kopecek, K. Peter, and P. Fath, "Crystalline silicon solar cells with selective emitter for industrial mass production," in *24th European Photovoltaic Solar Energy Conference*, Hamburg, Germany, 2009, pp. 1068-1071.

[50] R. J. Low, A. Gupta, N. P. Baterman, D. Ramappa, P. Sullivan, W. Skinner, J. Mullin, S. Peters, and H. Weiss-Wallrath, "High efficiency selective emitter cells enabled through patterned ion implantation," in *35th IEEE Photovoltaic Specialists Conference*, Honolulu, USA, 2010, pp. 1924-1928.

[51] H. Haverkamp, A. Dastgheib-Shirazi, B. Raabe, F. Book, and G. Hahn, "Minimizing the electrical losses on the front side: development of a selective emitter process from a single diffusion," in *33rd IEEE Photovoltaic Specialists Conference*, Diego, USA, 2008, pp. 1-4.

[52] S. J. Eisele, T. C. Ro¨der, J. R. Ko¨hler, and J. H. Werner, "18.9% efficient full area laser doped silicon solar cell," *Appl. Phys. Lett.*, vol. 95, p. 133501, 2009.

[53] T. C. Ro¨der, S. J. Eisele, P. Grabitz, C. Wagner, G. Kulushich, J. R. Ko¨hler, and J. H. Werner, "Add-on laser tailored selective emitter solar cells," *Prog. Photovolt. Res. Appl. ,* vol. 18, pp. 505–510, 2010.

[54] D. Kray, N. Bay, G. Cimiotti, S. Kleinschmidt, N. Ko¨sterke, A. Lo¨sel, M. Sailer, A. Tra¨ger, H. Ku¨hnlein, H. Nussbaumer, C. Fleischmann, and F. Granek, "Industrial LCP selective emitter solar cells with plated contacts," in *35th IEEE Photovoltaic Specialists Conference*, Honolulu, USA, 2010, pp. 667-671.

[55] B. S. Tjahjono, V. Wu, H. T. Anditsch, J. Cheng, J. Ting, M. J. Yang, T. Sziptalak, B. Beilby, and K. C. Hsu, "Optimizing selective emitter technology in one year of full scale production," in *26th European Photovoltaic Solar Energy Conference*, Hamburg, Germany, 2011, pp. 901–905.

[56] B. S. Tjahjono, M. J. Yang, C. Y. Lan, J. Ting, A. Sugianto, H. Ho, N. Kuepper, B. Beilby, T. Szpitalak, and S. R. Wenham, "18.9% efficient laser doped selective emitter solar cell on industrial grade p-type czochralski wafer," in *25th European Photovoltaic Solar Energy Conference*, Valencia, Spain, 2010, pp. 1396–1400.

[57] G. Hahn, "Status of Selective Emitter Technologies," in *25th European Photovoltaic Solar Energy Conference and Exhibition/5th World Conference on Photovoltaic Energy Conversion*, Valencia, 2010, p. 1091.

[58] H. Jin and K. J. Weber, "Relationship between interface defect density and surface recombination velocity in (111) and (100) Silicon / Silicon Oxide structure," in *23rd European Photovoltaic Solar Energy Conference*, Valencia, Spain, 2008, pp. 244-247.

[59] J. Benick, A. Leimenstoll, and O. Schultzm, "Comprehensive studies of passivation quality on boron diffused silicon surfaces," in *22nd European Photovoltaic Solar Energy Conference*, Milano, Italy, 2007, pp. 1244-1247.

[60] M. A. Green, A. W. Blakers, J. Zhao, A. M. Milne, A. Wang, and X. Dai, "Characterization of 23-percent efficient silicon solar cells," *IEEE Trans. Electron Devices*, vol. 37, pp. 331-336, 1990.

[61] J. H. Lai, A. Upadhyaya, S. Ramanathan, A. Das, K. Tate, V. Upadhyaya, A. Kapoor, C. W. Chen, and A. Rohatgi, "High-Efficiency Large-Area Rear Passivated Silicon Solar Cells With Local Al-BSF and Screen-Printed Contacts," *IEEE Journal of Photovoltaics*, vol. 1, pp. 16-21, 2011.

[62] H. Robbins and B. Schwartz, "Chemical etching of Silicon I," *Journal of Electrochemical Society*, vol. 106, pp. 505-508, 1959.

[63] G. Kästner, M. Zimmer, K. Birmann, F. M. M. Souren, J. Rentsch, and R. Preu, "Single side polish etching for the rear side of crystalline silicon wafers," in *25th European Photovoltaic Solar Energy Conference and Exhibition/ 5th World Conference on Photovoltaic Energy Conversion*, Valencia, 2010, pp. 2055-2058.

[64] R. Preu, A. Wolf, M. Hofmann, F. Clement, J. Nekarda, J. Rentsch, and D. Biro, "Challenges and advances in back-side metallization," *Photovoltaics International*, vol. 7, pp. 64-75, 2010.

[65] R. R. King, R. A. Sinton, and R. M. Swanson, "Low surface recombination velocities on doped silicon and their implications for point contact solar cells," in *19th IEEE Photovoltaic Specialists Conference*, New Orleans, 1987, pp. 1168-1173.

[66] M. J. Kerr and A. Cuevas, "Very low bulk and surface recombination in oxidized silicon wafers," *SEMICONDUCTOR SCIENCE AND TECHNOLOGY*, vol. 17, pp. 35-38, 2002.

[67] T. Lauinger, J. Schmidt, A. G. Aberle, and R. Hezel, "Record low surface recombination velocities on 1 Ω cm p-silicon using remote plasma silicon nitride passivation," *Applied Physics Letters*, vol. 68, p. 1232, 1996.

[68] O. Schultz, M. Hofmann, S. W. Glunz, and G. P. Willeke, "Silicon oxide/silicon nitride stack system for 20% efficient silicon solar cells," in *31st IEEE Photovoltaic Specialists Conference*, Florida, 2005, pp. 872- 876.

[69] B. Hoex, S. B. S. Heil, E. Langereis, M. C. M. van de Sanden, and W. M. M. Kessels, "Ultralow surface recombination of c-Si substrates passivated by plasma-

assisted atomic layer deposited Al[sub 2]O[sub 3]," *Applied Physics Letters*, vol. 89, p. 042112, 2006.

[70] B. Hoex, J. Schmidt, R. Bock, P. P. Altermatt, M. C. M. van de Sanden, and W. M. M. Kessels, "Excellent passivation of highly doped p-type Si surfaces by the negative-charge-dielectric Al[sub 2]O[sub 3]," *Applied Physics Letters*, vol. 91, p. 112107, 2007.

[71] B. Hoex, J. J. H. Gielis, M. C. M. van de Sanden, and W. M. M. Kessels, "On the c-Si surface passivation mechanism by the negative-charge-dielectric Al[sub 2]O[sub 3]," *Journal of Applied Physics*, vol. 104, p. 113703, 2008.

[72] G. Agostinelli, A. Delabie, P. Vitanov, Z. Alexieva, H. F. W. Dekkers, S. De Wolf, and G. Beaucarne, "Very low surface recombination velocities on p-type silicon wafers passivated with a dielectric with fixed negative charge," *Solar Energy Materials and Solar Cells*, vol. 90, pp. 3438-3443, 2006.

[73] J. Schmidt, A. Merkle, R. Brendel, B. Hoex, M. C. M. v. de Sanden, and W. M. M. Kessels, "Surface passivation of high-efficiency silicon solar cells by atomic-layer-deposited Al2O3," *Progress in Photovoltaics: Research and Applications*, vol. 16, pp. 461-466, 2008.

[74] E. Schneiderlochner, R. Preu, R. Ludemann, S. W. Glunz, and a. G. Willeke, "Laser-fired contacts (LFC)," in *17th European Photovoltaic Solar Energy Conference*, Munich, Germany, 2001, pp. 1303-1305.

[75] P. Ortega, G. Lopez, A. Orpella, I. Martin, M. Colina, C. Voz, S. Bermejo, J. Puigdollers, M. Garcia, and R. Alcubilla, "Crystalline silicon solar cells beyond 20% efficiency," in *Spanish Conference on Electron Devices*, Palma de Mallorca, 2011, pp. 1-4.

[76] S. Mack, U. Jäger, G. Kästner, E. A. Wotke, U. Belledin, A. Wolf, R. Preu, and D. Biro, "Towards 19% efficient industrial PERC devices using simultaneous front emitter and rear surface passivation by thermal oxidation," in *35th IEEE Photovoltaic Specialists Conference*, Honolulu, Hawaii, USA, 2010, pp. 34-38.

[77] M. Hofmann, P. Saint-Cast, D. Suwito, J. Seiffe, C. Schmidt, S. Kambor, L. Gautero, N. Kohn, J.-F. Nekarda, A. Leimenstoll, D. Wagenmann, D. Erath, J. Catoir, W. Wolke, S. Janz, D. Biro, A. Grohe, J. Rentsch, S. W. Glunz, and R. Preu, "Overview on crystalline silicon solar cells using PECVD rear passivation and laser-fired contacts," in *24th European Photovoltaic Solar Energy Conference*, Hamburg, Germany, 2009, pp. 1517-1522.

[78] T. Böscke, R. Hellriegel, T. Wütherich, L. Bornschein, A. Helbig, R. Carl, M. Dupke, D. Stichtenoth, T. Aichele, R. Jesswein, T. Roth, C. Schöllhorn, T. Geppert, A. Grohe, J. Lossen, and K. H.-J., "Fully Screen-Printed PERC Cells with Laser-Fired-Contacts - an Industrual Cell Concept with 19.5% Efficiency," in *37th IEEE Photovoltaic Specialists Conference*, Seattle, USA, 2011, pp. 3663-3666.

[79] J. Nekarda, S. Stumpp, L. Gautero, M. Hörteis, A. Grohe, D. Biro, and R. Preu, "LFC on screen printed aluminium rear side metallization," in *24th European Photovoltaic Solar Energy Conference*, Hamburg, Germany, 2009, pp. 1411-1415.

[80] S. Mack, U. Jäger, A. Wolf, S. Nold, R. Preu, and D. Biro, "Simultaneous front emitter and rear surface passivation by thermal oxidation - an industrially feasible

approach to a 19% efficient PERC device," in *25th European Photovoltaic Solar Energy Conference*, Valencia, Spain, pp. 2218-2222.

[81] E. Urrejola, K. Peter, H. Plagwitz, and G. Schubert, "Silicon diffusion in aluminum for rear passivated solar cells," *Appl. Phys. Lett.* , vol. 98, p. 153508, 2011.

[82] S. Ramanathan, A. Das, I. B. Cooper, A. Rohatgi, A. Payne, and I. Koehler, "20% efficient screen printed LBSF cell fabricated using UV laser for rear dielectric removal," in *35th IEEE Photovoltaic Specialists Conference*, Honolulu, HI, 2010, pp. 678-682.

[83] S. Ramanathan, "Understanding and development of dielectric passivated high efficiency silicon solar cells using spin-on solutions," Ph.D., Georgia Institute of Technology, 2012.

[84] D. Erath, A. Filipovic, M. Retzlaff, A. K. Goetz, F. Clement, D. Biro, and R. Preu, "Advanced screen printing technique for high definition front side metallization of crystalline silicon solar cells," *Solar Energy Materials and Solar Cells*, vol. 94, pp. 57-61, 2010.

[85] B.Raabe, F. Huster, M. McCann, and P. Fath, "High aspect ratio screen printed fingers," in *20th European Photovoltaic Solar Energy Conference*, Barcelona, Spain, 2005.

[86] E. Reis, D. Huljić, P. Hahne, R.Preu, D.Zickermann, B. Bucher, and P. V. Fleischer, "Fine-line screen printing for solar cells," in *11th International Photovoltaic Science and Engineering Conference*, Hokkaido, Japan, 1999, pp. 335-336.

[87] T. Kaydanova, M. F. A. M. van Hest, A. Miedaner, C. J. Curtis, J. L. Alleman, M. S. Dabney, E. Garnett, S. Shaheen, L. Smith, R. Collins, J. I. Hanoka, A. M. Gabor, and D. S. Ginley, "Direct Write Contacts for Solar Cells," in *31st IEEE Photovoltaic Specialists Conference*, Florida, 2005, pp. 1305-1308.

[88] K. F. Teng and R. W. Vest, "Application of Ink Jet Technology on Photovoltaic metallization," *IEEE Electron Device Letters*, vol. 9, pp. 591- 593 1988.

[89] R. A. Sinton and A. Cuevas, "Contactless determination of current–voltage characteristics and minority-carrier lifetimes in semiconductors from quasi-steady-state photoconductance data," *Applied Physics Letters*, vol. 69, p. 2510, 1996.

[90] R. A. Sinton and A. Cuevas, "A quasi-steady-state open-circuit voltage method for solar cell characterization," in *16th European Photovoltaic Solar Energy Conference*, Glasgow, Scotland, 2000, pp. pp. 1152–1155.

[91] P. A. Basore, "Numerical modeling of textured silicon solar cells using PC-1D," *IEEE Trans. Electron Devices*, vol. 37, pp. 337-343, 1990.

[92] P. A. Basore, "Extended spectral analysis of internal quantum efficiency," in *23rd IEEE Photovoltaic Specialists Conference*, Louisville, Kentucky, 1993, pp. 147 - 152.

[93] D. E. Kane and R. M. Swanson, "Measurement of the emitter saturation current by a contactless photoconductivity decay method," in *18th IEEE Photovoltaic Specialists Conference*, Las Vegas, Nevada, 1985, pp. 578-583.

[94] T. Fellmeth, A. Born, A. Kimmerle, F. Clement, D. Biro, and R. Preu, "Recombination at metal emitter interfaces of front contact technologies for highly efficient silicon solar cells," *Energy Procedia,* vol. 8, pp. 115-121, 2011.
[95] "Analyst Reaction - Solar Price Surveys," Bloomberg New Energy Finance2013.
[96] E. C. Douglas and R. V. D'Aiello, "A study of the factors which control the efficiency of ion-implanted silicon solar cells," *IEEE Transactions on Electron Devices,* vol. 27, pp. 792-802 1980.
[97] M. B. Spitzer, S. P. Tobin, and C. J. Keavney, "High-efficiency ion-implanted silicon solar cells," *IEEE Transactions on Electron Devices,* vol. 31, pp. 546-550, 1984.
[98] P. R. Younger and S. N. Bunker, "Ion implantation processing for high performance concentrator solar cells and cell assemblies," *Solar Cells,* vol. 6, pp. 79-86, 1982.
[99] A. Rohatgi, D. L. Meier, B. McPherson, Y.-W. Ok, A. D. Upadhyaya, J.-H. L. Lai, and F. Zimbardi, "High-throughput ion-implantation for low-cost high-efficiency silicon solar cells," *Energy Procedia,* vol. 15, pp. 10-19, 2012.
[100] K. Chundrui. (2010, August) Implants for better cells? *PHOTON International*. 68-70.
[101] E. Peiner, A. Schlachetzki, and D. Krüger, "Doping profile analysis in Si by electrochemical capacitance-voltage measurements," *Journal of Electrochemical Society,* vol. 142, pp. 576-580, 1995.
[102] S. Dauwe, L. Mittelstadt, A. Metz, and R. Hezel, "Experimental evidence of parasitic shunting in silicon nitride rear surface passivated solar cells," *Progress in Photovoltaics: Research and Applications,* vol. 10, pp. 271-278, 2002.
[103] T. Krygowski and A. Rohatgi, "A novel processing technology for high-efficiency silicon solar cells," *J. Electrochem. Soc.,* vol. 3, pp. 1141-1146, 1999.
[104] S. Ramanathan, V. Meemonqkotkiat, A. Das, A. Rohatgi, and I. Koehler, "Fabrication of 20% efficient cells using spin-on based simultaneous diffusion and dielectric anneal," in *34th IEEE Photovoltaic Specialists Conference*, Philadelphia, USA, 2009, pp. 2150-2153.
[105] SemiTest. (1998). *SCA-2500 surface charge analyzer user manual*.
[106] C. F. J. Wu and M. S. Hamada, *Experiments: Planning, Analysis, and Optimization*: Wiley, 2009.
[107] M. Inc. (1992). *Minitab reference manual*.
[108] X. Chen, K. Church, H. Yang, I. B. Cooper, and A. Rohatgi, "High aspect ratio fine gridline for front side metallization of industrial silicon solar cells by direct printing," in *26th European Photovoltaic Solar Energy Conference And Exhibition*, Hamburg, Germany, 2011, pp. 1094-1098.
[109] X. Chen, K. Church, H. Yang, I. B. Cooper, and A. Rohatgi, "Improved front side metallization for silicon solar cells by direct printing," in *37th IEEE Photovoltaic Specialists Conference*, Seattle,USA, 2011, pp. 3667-3671.
[110] D. L. Meier and S. D. K., "Contact resistance: its measurement and relative importance to power loss in a solar cell," *IEEE Trans. Electron Dev.* , pp. 647-653, 1984.
[111] I. B. Cooper, A. Ebong, J. S. Renshaw, R. Reedy, M. Al-Jassim, and A. Rohatgi, "Understanding and use of IR belt furnace for rapid thermal firing of screen-

printed contact to Si solar cells," *IEEE Electron Dev. Lett.,* vol. 31, pp. 461-463, 2010.

[112] D. L. Meier, E. A. Good, A. Garcia, B. L. Bingham, S. Yamanaka, V. Chandrasekaran, and C. Buchner, "Determining components of series resistance from measurements on a finished cell," in *IEEE 4th World Conference Photovoltaic Energy Conversion*, Waikoloa, USA, 2006, pp. 1315-1318.

[113] Y.-W. Ok, A. D. Upadhyaya, Y. Tao, F. Zimbardi, K. Ryu, M.-H. Kang, and A. Rohatgi, "Ion-implanted and screen-printed large area 20% efficient N-type front junction Si solar cells," *Solar Energy Materials and SolarCells,* vol. 123, pp. 92-96, 2014.

[114] V. T. Daudrix, J. Guillet, F. Freitas, A. Shah, C. Baliff, P. Winkler, M. Ferreloc, S. Bengali, X. Niquille, D. Fischer, and R. Morf, "Characterisation of rough reflecting substrates incorporated into thin-film slicon solar cells," *Prog. Photovoltaics,* vol. 14, pp. 485-498, 2006.

[115] N. Taneda, T. Oyama, and K. Sato, "Light scattering effects effect of highly textured trabsparent comductive [sic] oxides films," in *Tech. Digest 17th I-PVSEC, Toyota Technological Institute*, Fukuoka, Japan, 2007, pp. 309-310.

[116] H. Sai, H. Fujiwara, and M. Kondo, "Back surface reflector with periodic textures fabricated by self-ordering process for light trapping in microcrystalline silicon solar cells," in *Tech. Digest 17th I-PVSEC, Toyota Technological Institute*, Fukuoka, Japan, 2007, pp. 315-136.

[117] O. Berger, D. Inns, and A. G. Aberle, "Commercial white paint as back surface reflector for thin-film solar cells," *Sol. Energy Mater. Sol. Cells,* vol. 91, pp. 1215-1221, 2007.

[118] J. E. Cotter, "Optical intensity of light in layers of silicon with rear diffuse reflectors," *J. Appl. Phys.*, vol. 84, pp. 618-624, 1998.

[119] A. Das and A. Rohatg, "Optical and electrical characterization of silver microflake colloid films," *Journal of Electrochemical Society,* vol. 157, pp. 301-303, 2010.

[120] D. L. Meier, V. Chandrasekaran, A. Gupta, V. Yelundur, and A. Rohatg, "Silver contact grid: inferred contactresistivity and cost minimization in 19% silicon solar cells," *IEEE journal of Photovoltaics,* vol. 3, pp. 199-205, 2013.

[121] S. W. Glunz, S. Rein, W. Warta, J. Knobloch, and W. Wettling, "On the Degradation of Cz-Silicon Solar Cells," in *2nd World Conference on Photovoltaic Solar Energy Conversion*, Vienna, Austria, 1998, pp. 1343-1346.

[122] A. Das and A. Rohatgi, "The impact of cell design on light induced degradation in p-type silicon solar cells," in *37th IEEE Photovoltaic Specialists Conference*, 2011, pp. 158-164.

[123] K. Bothe, R. Hezel, and J. Schmidt, "Recombination-Enhanced Formation of the Metastable Boron–Oxygen Complex in Crystalline Silicon," *Appl. Phys. Lett.,* vol. 83, pp. 1125-1127, 2003.

[124] J. Schmidt and K. Bothe, "Structure and transformation of the metastable boron- and oxygen-related defect center in crystalline silicon," *Phys. Rev. B,* vol. 69, p. 024107, 2004.

[125] K. Bothe, R. Sinton, and J. Schmidt, "Fundamental boron–oxygen-related carrier lifetime limit in mono- and multicrystalline silicon," *Prog. Photovolt.: Rev. and Appl.,* vol. 13, pp. 287-296, 2005.
[126] S. W. Glunz, B. Köster, T. Leimenstoll, S. Rein, E. Schäffer, J. Knobloch, and T. Abe, "100 cm2 solar cells on Czochralski silicon with an efficiency of 20.2%," *Prog. Photovolt.: Res. and Appl.,* vol. 8, pp. 237-240, 2000.
[127] V. Meemongkolkiat, K. Nakayashiki, A. Rohatgi, G. Crabtree, J. Nickerson, and T. L. Jester, "The effect of the variation in resistivity and lifetime on the solar cells performance along the commercially grown Ga- and B-doped Czochralski ingots," in *31st IEEE Photovoltaic Specialists Conference*, Orlando, Florida, 2005, pp. 1115-1118.
[128] X. Yu, X. Zheng, K. Hoshikawa, and D. Yang, "Crystal growth of indium-doped czochralski silicon for photovoltaic application," *Jpn. J. Appl. Phys.*, vol. 51, p. 105501, 2012.
[129] T. W. Hicks, A. E. Organ, and N. Riley, "Oxygen transport in magnetic Czochralski growth of silicon with a non-uniform magnetic field," *Journal of Crystal Growth*, vol. 94, pp. 213-228, 1989.
[130] D. L. Meier, V. Chandrasekaran, A. Gupta, V. Yelundur, and A. Rohatgi, "Silver contact grid: inferred contact resistivity and cost minimization in 19% silicon solar cells," *IEEE Journal of Photovoltaics*, vol. 3, pp. 199-205, 2013.
[131] C.-W. Chen, M.-H. Kang, V. Upadhyaya, A. Kapoor, J. K. Tate, J. C. Keane, S. Ning, and A. Rohatgi, "Understanding and development of screen-printed front metallization for high-efficiency low-to-medium concentrator silicon solar cells," *IEEE Journal of Photovoltaics,* vol. 3, pp. 944-951, 2013.
[132] R. Woehl, P. Gundel, J. Krause, K. Ruhle, F. D. Heinz, M. Rauer, C. Schmiga, M. C. Schubert, W. Warta, and D. Biro, "Evaluating the aluminum-alloyed p+ -layer of silicon solar cells by emitter saturation density and optical microspectroscopy measurements," *IEEE Trans. Electron Devices,* vol. 58, pp. 441-447, 2011.

# PUBLICATION FROM THIS WORK


[1] **Jiun-Hong Lai**, Ajay Upadhyaya, Rishi Ramanathan, Arnab Das, Keith Tate, Vijaykumar Upadhyaya, Aditya Kapoor, Chai-Wei Chen, Ajeet Rohatgi, "High-Efficiency Large-Area Rear Passivated Silicon Solar Cells with Local Al BSF and Screen-Printed Contacts," *IEEE J. Photovoltaics*, vol. 1, pp16-21, 2011.

[2] Yuguo Tao, Young-Woo Ok , Francesco Zimbardi , Ajay D Upadhyaya, **Jiun-Hong Lai**, Steven Ning, Vijaykumar D Upadhyaya, Ajeet Rohatgi, "Fully Ion-implanted and Screen-printed 20.2% Efficient Front Junction Silicon Cells on 239cm2 Commercial N-type CZ Substrate," submitted to *IEEE J Photovoltaic*, 2013.

[3] A. Rohatgi, Brian Rounsaville, and **Jiun-Hong Lai**, Ning Duanmu, Scott Turchetti, Christine Richardson, Henry Chou, and Vikram Singh, "MonoCast™ Silicon's Potential for Commercially Viable High Efficiency Solar Cells," submitted to *Progress in Photovoltaics*, 2013.

[4] Ajeet Rohatgi, Daniel L. Meier, Bruce McPherson, Young-Woo Ok, Ajay D. Upadhyaya, **Jiun-Hong Lai**, Francesco Zimbardi, "High-Throughput Ion-Implantation for Low-Cost High-Efficiency Silicon Solar Cells," *Energy Procedia*, V. 15, 2012, pp. 10-19.

[5] J.-H. Lai, A.D. Upadhyaya, E. Cho, A. Rohatgi, M.J. Binns, J. Appel, J. Guo, H. Fang and E.A. Good, "Use of Indium Doping to Mitigate Light Induced Degradation in High Efficiency p-Type Silicon Solar Cells," *40th IEEE Photovoltaic Specialists Conference*, 2014.

[6] Yuguo Tao, Young-Woo Ok , Francesco Zimbardi , Ajay D Upadhyaya, **Jiun-Hong Lai**, Steven Ning, Vijaykumar D Upadhyaya, Ajeet Rohatgi, "Fully Ion-implanted and Screen-printed 20.2% Efficient Front Junction Silicon Cells on 239cm2 Commercial N-type CZ Substrate," *39th IEEE Photovoltaic Specialists Conference*, 2013.

[7] **Jiun-Hong Lai**, A. Upadhyaya, R. Ramanathan, A. Das, K. Tate, V. Upadhyaya, A. Kapoor, Chai-Wei Chen, A. Rohatgi, "Large Area 19.4% Efficient Rear Passivated Silicon Solar Cells With Local Al BSF and Screen-Printed Contacts," *37th IEEE Photovoltaic Specialists Conference*, 2011, pp. 1929.

[8] **Jiun-Hong Lai**, Ian B. Cooper, Xudong Chen, Kenneth Church, Haixin Yang, Ajeet Rohatg, "Large-Area ~20% Efficient Silicon Solar Cells Using Fine Line Direct Printing," *38th IEEE Photovoltaic Specialists Conference*, 2012, pp. 2192-2195.

[9] Ajeet Rohatgi, Daniel L. Meier, Bruce McPherson, Young-Woo Ok,; Ajay D. Upadhyaya, **Jiun-Hong Lai**, Francesco Zimbardi, "High-Throughput Ion-implantation for Low-Cost High-Efficiency Silicon Solar Cells," *6th International Conference on Materials for Advanced Technologies*, 2011, pp. 10-19.

[10] A. Upadhyaya, V. Yelundur, S. Ramanathan, **Jiun-Hong Lai**, V. Upadhyaya, A. Rohatgi, A, I. Koehler, "Enhanced Front and Rear Dielectric Passivation for Commercially Grown Czochralski Silicon for High Efficiency Solar Cells," *34th IEEE Photovoltaic Specialists Conference*, 2009, pp. 1754-1757.

# VITA

## JIUN-HONG LAI

Jiun-Hong Lai received his B.S. degree in Electrical Engineering from Chung-Hua University, Hsinchu, Taiwan, in 1996, and his M.S. degree in Electrical and Control engineering from National Chiao-Tung University, Hsinchu, Taiwan, in 1997. He received another M.S. degree from the Georgia Institute of Technology in 2010. In 2009, he joined the University Center of Excellence for Photovoltaics (UCEP) at the Georgia Institute of Technology, where he is currently pursuing the Doctor of Philosophy degree in Electrical Engineering under the supervision of Dr. Ajeet Rohatgi.

Upon graduating early from graduate school in 1997, he was with the Department of Bio-Industrial Mechatronics Engineering, National Taiwan University, where he was a research assistant engaged in researching the analysis of environmental condition control for cabbage seedling growth. After two years of military service in 2000, he was a principle engineer at the Taiwan Semiconductor Manufacturing Company for seven years. He was responsible for developing a control system for the gate formation of semiconductor devices. He was awarded two patents in the field of advanced process control. From 2007 to 2008, he was a graduate research assistant for the Gigascale Integration Group of the Microelectronics Research Center at the Georgia Institute of Technology. He was working in the area of 3-D electronic interconnection systems under the supervision of Dr. Muhannad S. Bakir and Dr. James D. Meindl. In 2009, he joined UCEP group, where he is pursuing his Ph.D. degree.

In 2011, he won the Best Student Paper Award at the 37$^{th}$ IEEE Photovoltaics Specialists Conference in Seattle. His research focuses on the design and the fabrication of commercial grade low-cost high-efficiency advanced silicon solar cells.